Vision only Sense and Avoid System

Zoltán Nagy
(MTA-SZTAKI, PPKE-ITK)

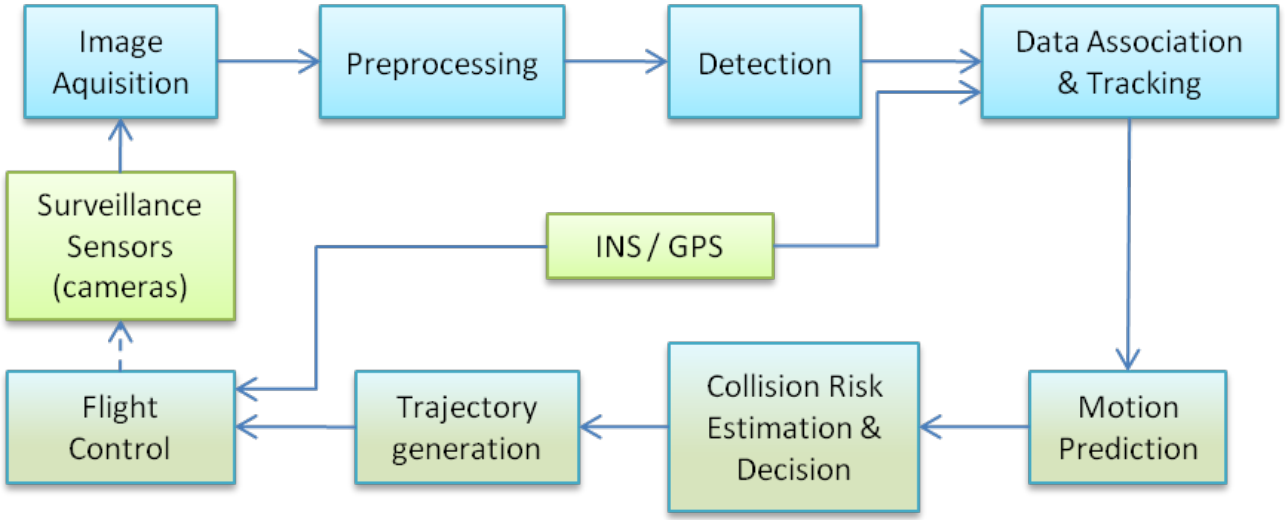
TÁMOP-4.2.2/B-10/1/2012-0014

Nemzeti Fejlesztési Ügynökség
www.ujszechenyiterv.gov.hu
06 40 638 638

MAGYARORSZÁG MEGÚJUL

A projekt az Európai Unió támogatásával valósul meg.

Vision only Sense and Avoid System

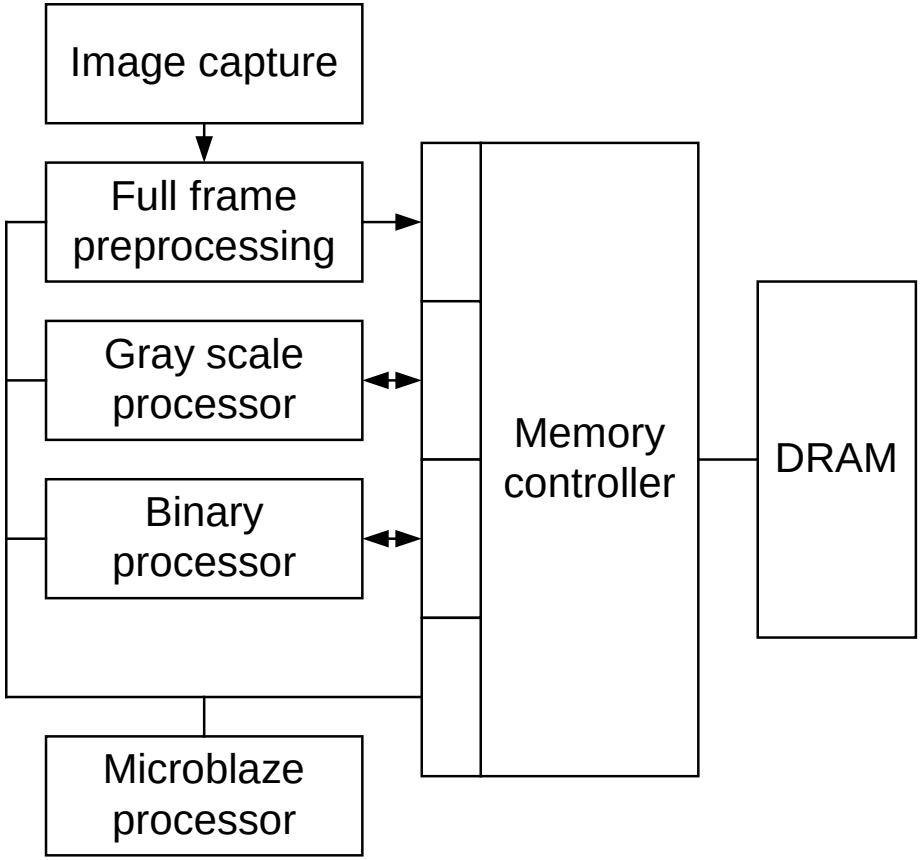


- Sensing Technology
  - Image processing with low power consumption
  - Megapixel resolution cameras for large FOV
- Estimation and Control
  - Low observability process
  - Guaranteed estimation precision
  - Trajectory generation for enhanced estimation

Synergy between low consumption many core computing units and advanced algorithms

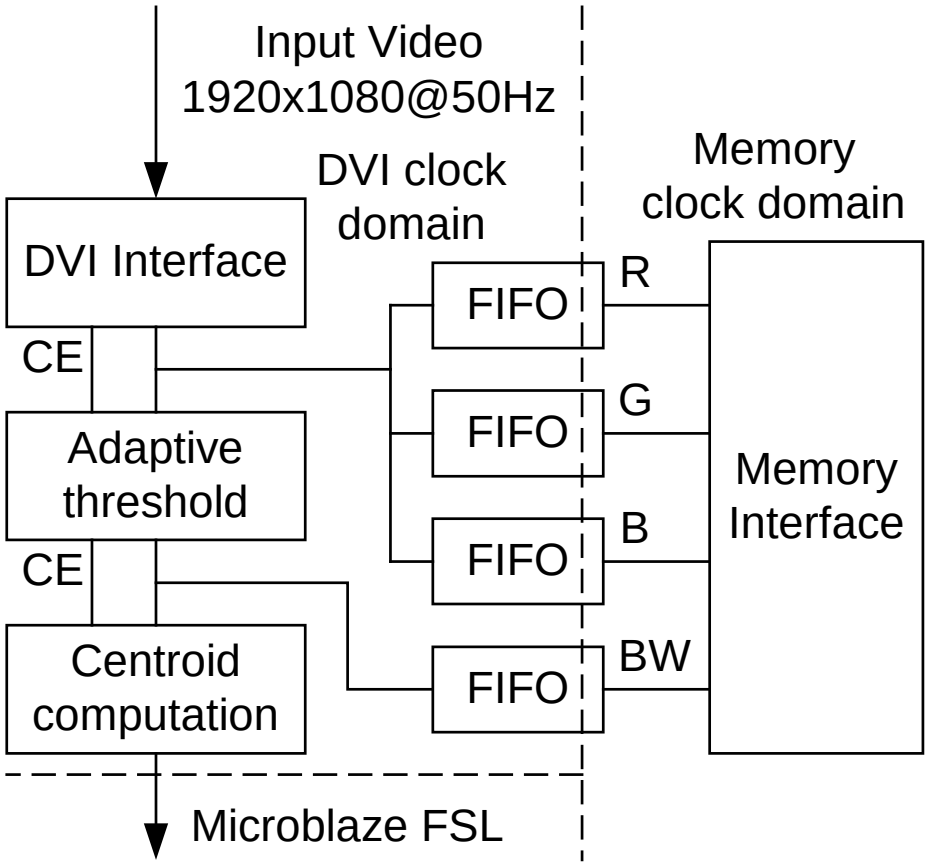
Image processing system

- Limited on-board payload
  - <250g
- Limited on-board power
  - <1W
- Input: DVI/HDMI
  - 1920x1080@50Hz
- Xilinx SP605 development system
  - XC6SLX45T-3 FPGA
  - 128MB DDR3 SDRAM
  - 10/100/1000 Ethernet
  - FMC-LPC connector



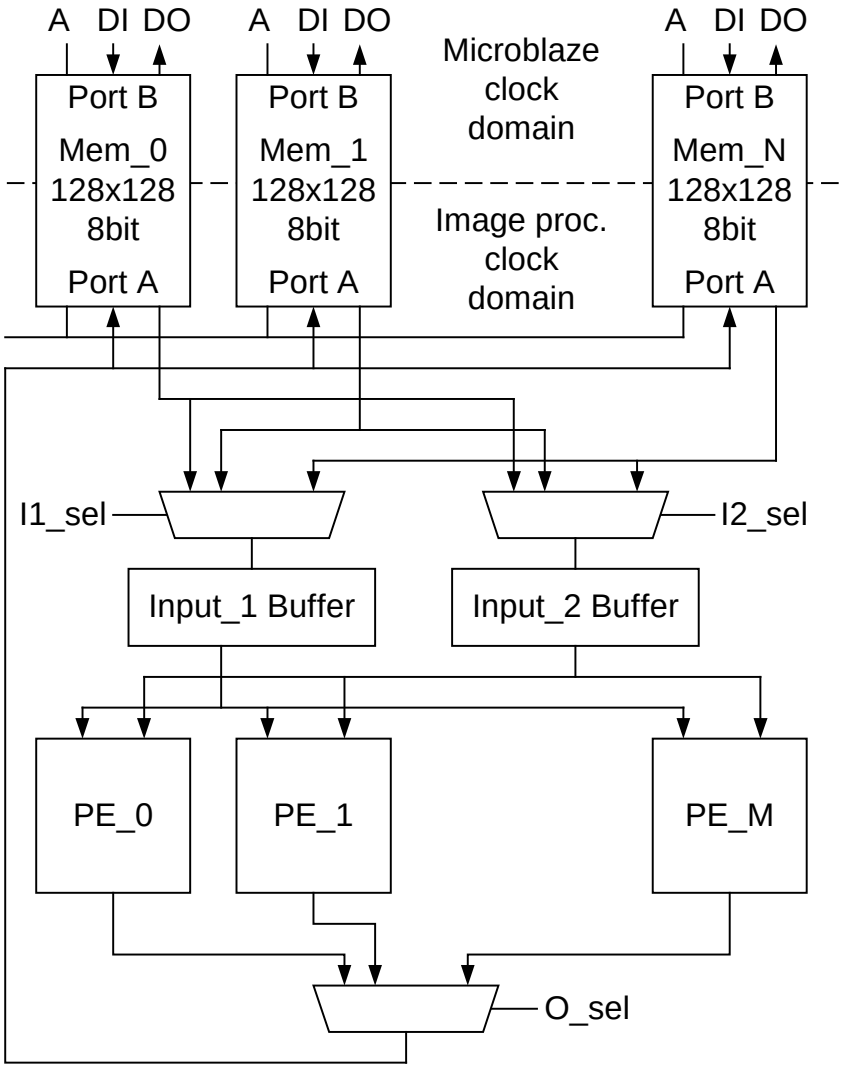
Full frame image preprocessor

- Adaptive threshold
  - 3x3, 5x5, 7x7 neighborhood
  - Programmable threshold level
- Centroid computation
  - 32x32 centroid
  - Final 128x128 centroid computed by Microblaze



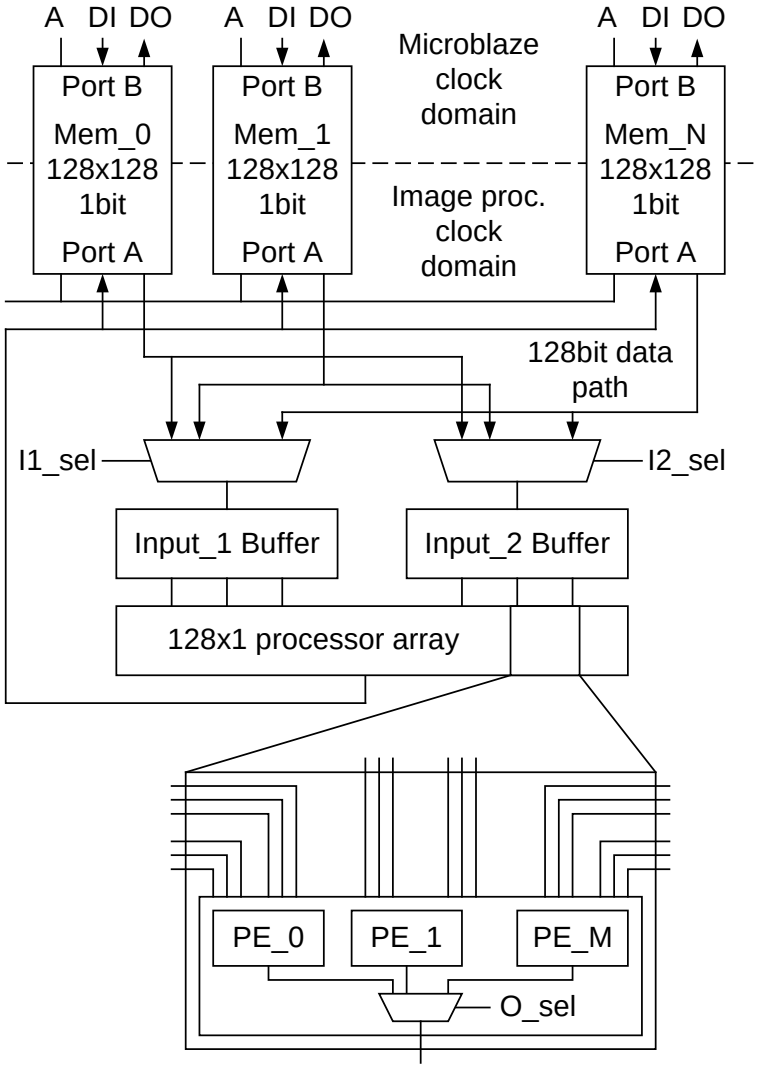
Gray scale processor

- On-chip memories
  - 128x128 pixel images
  - 8 RAMB18
  - Separate port for fast Microblaze access
- Separate clock domain
- Specialized Processing Elements (PE)
- Supported operations:
  - Edge Average, Diffusion, Threshold, Pixel wise arithmetic operations
  - Global white, black, change
- Expected performance:
  - 150MHz, 110us/op, 9100op/s



Binary processor

- On-chip memories
  - 128x128 pixel images
  - 1 RAMB18
  - Separate port for fast Microblaze access
- Separate clock domain
- One line of Specialized Processing Elements (PE)
- Supported operations:
  - Erosion, Dilation, Recall, Pixel wise logic operations
  - Global white, black, change
- Expected performance:
  - 150MHz, 0.85us/op, 1,171,875op/s



Extended Kalman filter

$$x_k = A_{k-1}x_{k-1} + B_{k-1}u_{k-1} + v_{k-1}$$
$$y_k = C_k x_k + z_k$$

$$E\{x(0)\} = \hat{x}_0,\ E\{(x(0) - \hat{x}_0)(x(0) - \hat{x}_0)^T\} = \Sigma_0$$
$$E\{v_k\} = 0,\ E\{v_k v_k^T\} = R_{kv},\ E\{v_k v_j^T\} = 0, j \neq k$$
$$E\{z_k\} = 0,\ E\{z_k z_k^T\} = R_{kz},\ E\{z_k z_j^T\} = 0, j \neq k$$
$$E\{z_k v_j^T\} = 0, \forall j, k$$

Time update:

$$\bar{x}_k = A_{k-1}\hat{x}_{k-1} + B_{k-1}u_{k-1}$$
$$M_k = A_{k-1}\Sigma_{k-1}A_{k-1}^T + R_{k-1,v}$$

Feedback gain:

$$G_k = \Sigma_k C_k^T R_{kz}^{-1}$$

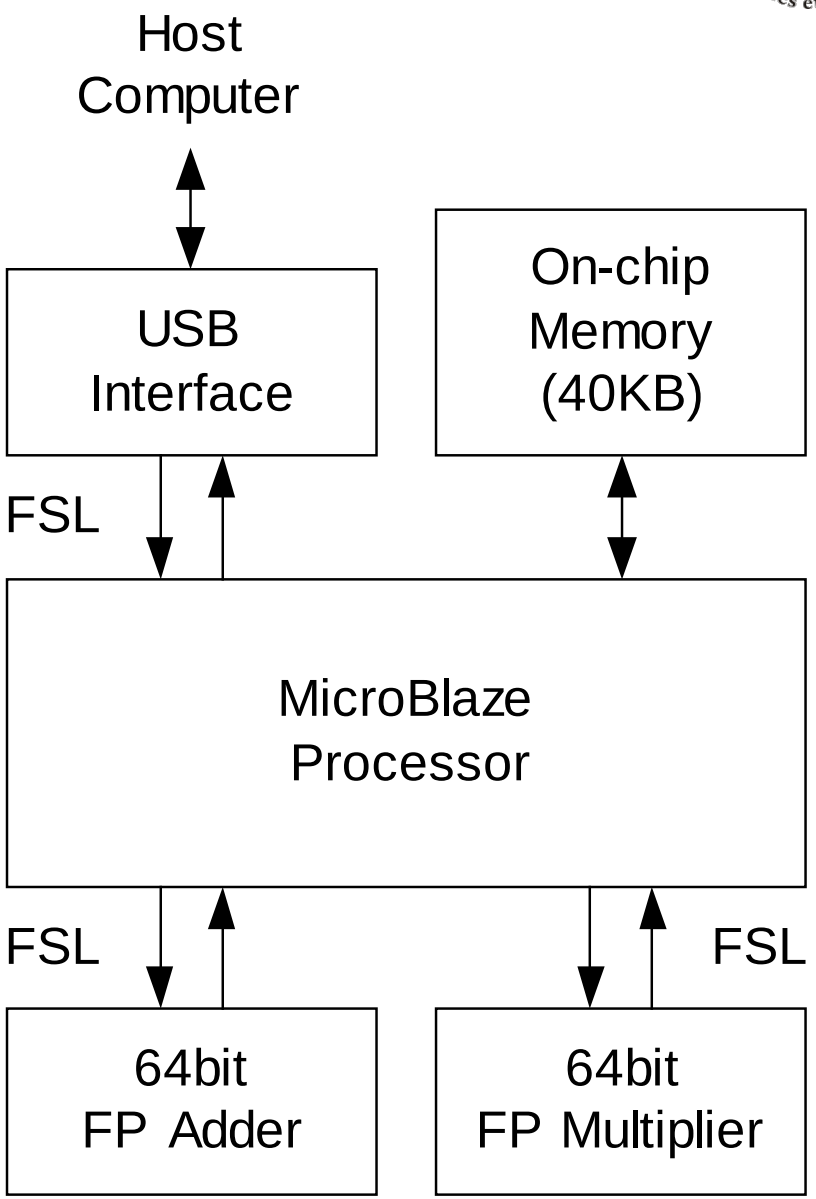
Measurement update:

$$\hat{x}_k = \bar{x}_k + G_k(y_k - C_k\bar{x}_k)$$
$$\Sigma_k = M_k - M_k C_k^T (C_k M_k C_k^T + R_{kz})^{-1} C_k M_k$$

- Matrix-vector operations
- Matrix inversion
- Microcontrollers
  - limited performance
  - 32bit floating point support only

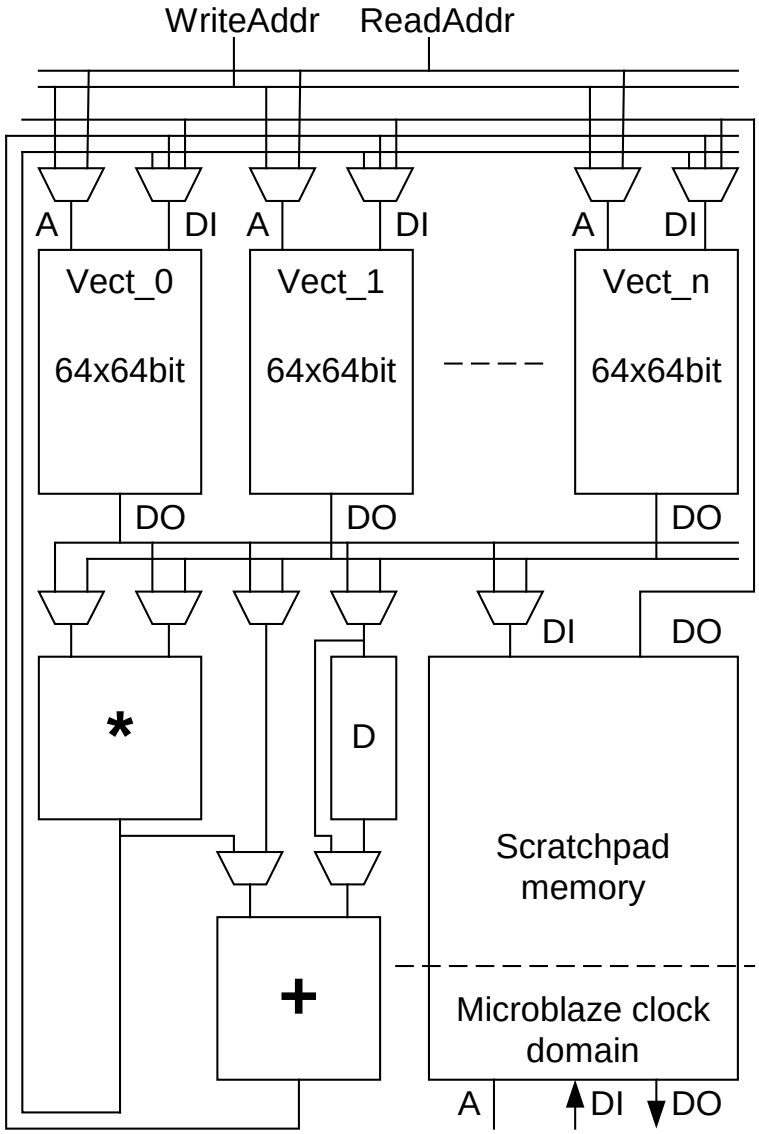
Implementation

- Xilinx MicroBlaze soft-processor core
  - 32bit floating point unit
  - 64bit floating point software library
- Hardware accelerators
  - 64bit floating point adder
  - 64bit floating point multiplier

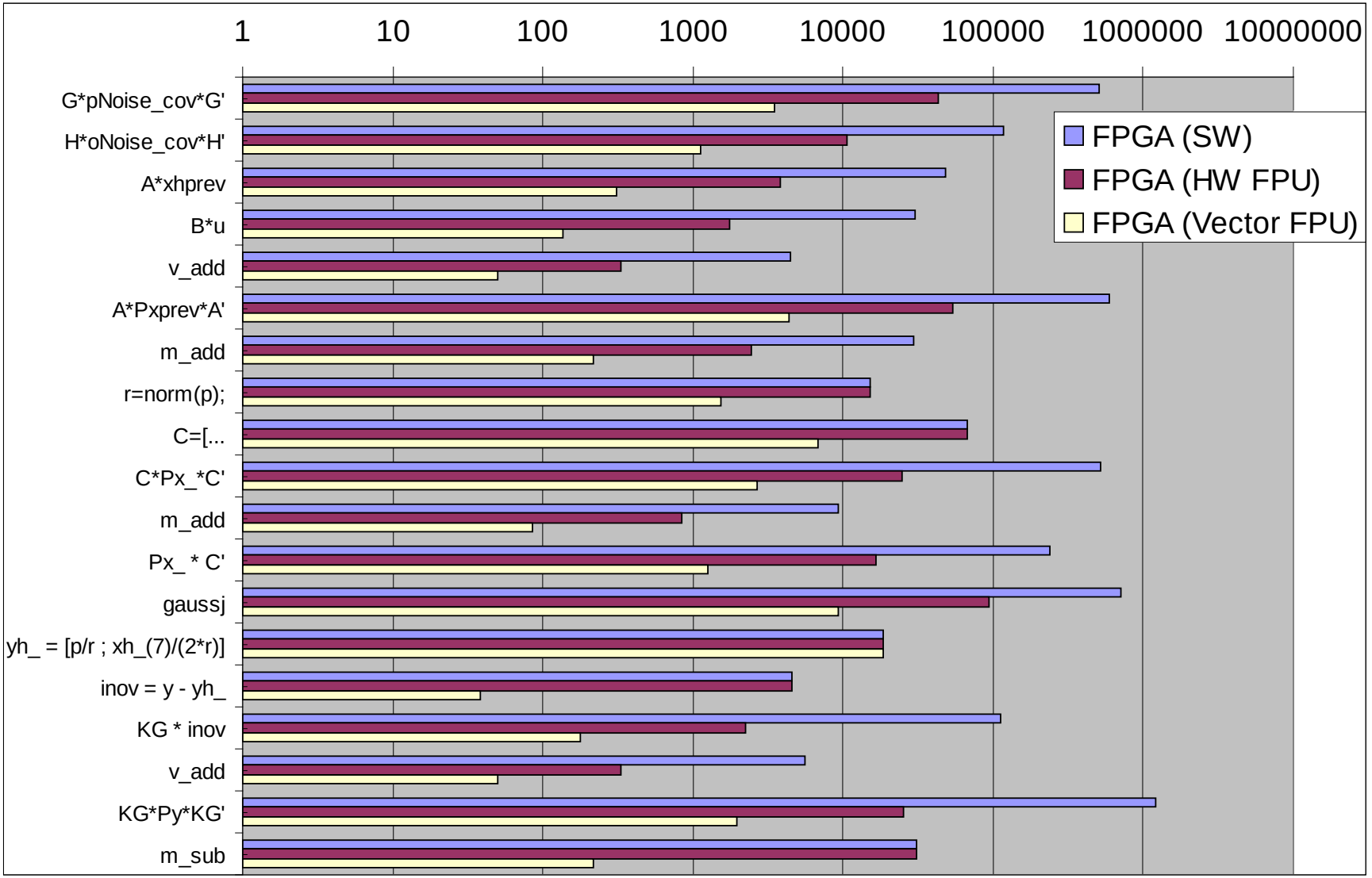


Vector unit for Kalman filter

- On-chip memories
  - Scratchpad memory
  - Separate port for fast Microblaze access
  - 64bit wide 64 element vector registers
- Configurable vector length
- Separate clock domain
- 64bit double precision floating point units
- Supported operations:
  - Independent multiplication and addition
  - Multiply and add (MADD)



Profiling


1
10
100
1000
10000
100000
1000000
10000000
G*pNoise_cov*G'
H*oNoise_cov*H'
A*xhprev
B*u
v_add
A*Pxprev*A'
m_add
r=norm(p);
C=[...
C*Px_*C'
m_add
Px_ * C'
gaussj
yh_ = [p/r ; xh_(7)/(2*r)]
inov = y - yh_
KG * inov
v_add
KG*Py*KG'
m_sub
FPGA (SW)
FPGA (HW FPU)
FPGA (Vector FPU)

Speed

- Clock frequency: 50MHz (max. 150MHz)
- Software
  - 10.3 iteration / s (with communication)
- Accelerated floating-point addition and multiplication
  - 92.5 iteration / s (with communication)
- Vector processor
  - 732 iteration / s (with communication)

Area and power

Module	Slice Reg	LUTs	LUTRAM	BRAM	DSP	Power (mW)
MCB_DDR3	1978	2172	45	0	0	195.98
Soft_TEMAC	2636	2452	109	6	0	5.48
image_proc_0	**1737**	**3388**	**66**	**16**	**0**	**9.73**
image_proc_gray_0	**604**	**622**	**100**	**32**	**2**	**4.62**
vector_proc_0	**976**	**1040**	**544**	**4**	**16**	**14.56**
microblaze_0	1056	1363	113	0	3	5.07
vga_in_ctrl_0	1751	1896	344	2	0	22.32
other	1421	1356	48	4	0	211.48
System total	**13580**	**15645**	**1417**	**68**	**21**	**680.72**
Spartan-6 XC6SLX45T	54320	27288	6408	116	58	
FPGA usage	25.00%	57.32%	22.11%	58.62%	36.21%	

Conclusions, future work

- Image processing architecture is elaborated
- Expected performance
  - Gray 180 operations/frame (50Hz)
  - Binary 23,000 operations/frame (50Hz)
  - Low-power Kalman filter implemented
- Expected performance
  - 14 iterations/frame (50Hz)
- Power consumption: 1303mW
  - Quiescent: 623mW, dynamic: 680mW
- Xilinx Zync-7000
  - Dual ARM Cortex-A9 processor system
  - More complex image processing algorithms
  - Less power consumption