Simulation of charging properties of MNOS structures with embedded semiconductor nanocrystals

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Abstract— **The effect of the oxide thickness and the depth, size and location of semiconductor nanocrystals are studied on the charging behaviour of MNOS non-volatile memory structures by the calculation of electron and hole tunneling probability to the nanocrystals or to the nitride conduction or valence band, respectively, and by the simulation of memory hysteresis behaviour.**

It is concluded for both MNOS structures that the optimal for charging behaviour tunnel oxide thickness is about 2 nm The presence of nanocrystals enhances the charge injection resulting in better performance, but for structures with thin tunnel oxide layer (below 3 nm) only, and if the nanocrystals are located close to the oxide/nitride interface. But in the case of very high tunneling probability, i.e., of high tunneling currents the system approaches eqilibrium and the memory behaviour collapses..

I. INTRODUCTION

It was obtained in our recent works that the presence of Si or Ge nanocrystals (NCs) enhanced the charge injection properties of MNOS (metal-nitride-oxide-silicon) structures [1-3]. For better understanding of the experimental results, the tunneling probability of electrons and holes to the nanocrystals and to the conduction or valence band of the nitride layer, respectively, has been calculated for MNOS structures with and without nanocrystals [4] by WKB approximation [5]. Using these probabilities the memory behaviour (the memory window, the memory hysteresis and the retention properties) can be simulated to understand the role of different parameters, namely of the composition and thickness of layers, of the potential barrier heights, of the presence, material and size of nanocrystals. In one of our recent works [6] the effect of layer thicknesses were studied on the memory hysteresis characteristics of MNOS structures without the presence of nanocrystals. In this paper some results of simulations extended to study the effect of presence and position of semiconductor nanocrystals on the memory hysteresis behaviour of MNOS structures are briefly presented and discussed. Although the calculations have been performed for MNOS structures, the obtained dependences are valid for SONOS (silicon-oxide-nitride-oxide-silicon) structures as well, as the presence of a capping oxide layer does not influence the charge injection directly.

II. SIMULATION

On the basis of WKB approximation [5], if the tunneling probability of a charge carrier through a potential barrier with arbitrary shape is much less than unity, it can be expressed as

$$P = \exp\left(-\frac{2}{\hbar} \int_{x_1}^{x_2} \sqrt{2m^*[U(x) - E]}dx \right) \qquad (1)$$

where P is the tunneling probability, x_1 and x_2 are the coordinates, where the electron enters and leaves the potential barrier (turning points), m^* is the effective mass of the electron, $\hbar$ is the Planck constant (devided by 2π), $U(x)$ is the potential energy as a function of coordinate, and E is the electron energy.

The band diagram of the MNOS structure used in the calculations is presented in Fig. 1 [5]. No image force lowering, band bending at the silicon surface, and

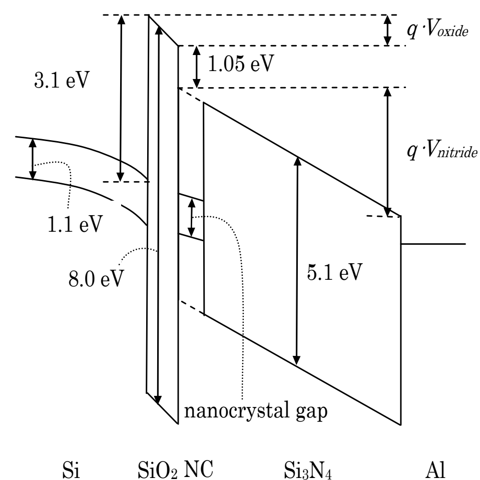

Figure 1. Band diagram of MNOS structures with (solid lines) and without (dashed lines) embedded semiconductor nanocrystals (NC) at the SiO_2/Si_3N_4 interface used for the calculations. The actual values of band gaps and discontinuities are taken from Ref. 5.

resonant tunneling have been considered. Intrinsic semiconductor nanocrystals were assumed, i.e., a constant electric field was considered within the nanocrystals.

For MNOS structures without nanocrystals the electron or hole tunneling was calculated to the nitride conductance or valence band, respectively. For structures with nanocrystals charge carriers can tunnel either directly to the nanocrystals and captured by them, or via the nanocrystals to the nitride conductance/valence band and captured by traps. The charging behaviour were calculated for both cases. For the second case a single step tunneling process was considered via the NCs to the nitride conduction/valence bands without capture and termalization of charge carriers in the nanocrystals, assuming a continuous energy state distribution in them.

The memory hysteresis were simulated by calculating the flat-band voltage shift due to the charge injected and stored in nanocrystals or in traps in the nitride layer. The net charge captured in nanocrystals or in the nitride layer during a voltage pulse, can be calculated by the integration of the difference of the current flowing into the structure via the oxide layer and that of flowing out of the structure via the nitride layer. The current via the oxide layer was obtained by the WKB approximation [5], while for current via the nitride our experimental results were used [7]. The details of integration is described elsewhere [6,8,9]. The hysteresis curves were begun to be calculated from zero pulse amplitude and zero flat-band voltage. For the simulation of hysteresis curves the voltage pulse amplitude was increased or decreased by 1 V step by step.

The effect of NCs was studied for oxide thickness range 0.1-5 nm, for a nitride thickness of 30 nm or 35 nm, and charge centroid of 6 nm. Nanocrystals with size in the range of 1-5 nm were considered either at the SiO_2/Si_3N_4 interface or located at a depth of 1-3 nm. The pulse width used for simulations was 10 ms.

III. RESULTS AND DISCUSSION

Fig. 2 presents the two extremes of electron tunneling probability to MNOS structures with or without embedded semiconductor nanocrystals as a function of the oxide thickness and the electric field in the oxide layer. It presents the tunneling probability to the conduction band of the nitride layer for MNOS structures with nanocrystals, if they are located deep in the nitride layer, deeper than the tunneling length, and either for MNOS structures without nanocrystals. The other extreme is the tunneling probability to the nanocrystals located at the SiO_2/Si_3N_4 interface. It is just the tunneling probability via the oxide layer. The tunneling probability via NCs or traps [10] located within the tunneling depth, is between these two extremes.

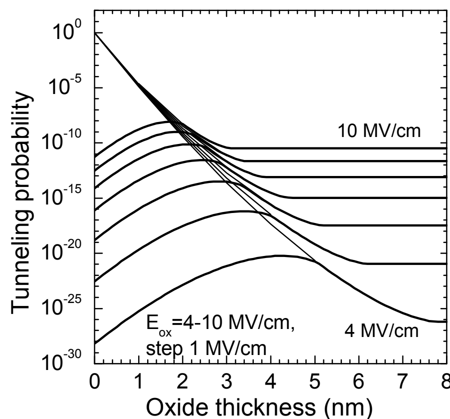

Figure 2. The two extremes of electron tunneling probability to MNOS structures with (thin lines) or without (thick lines) embedded semiconductor nanocrystals as a function of the oxide thickness and the electric field in the oxide layer.

The tunneling probability to the conductance band exhibits maximum as a function of oxide thickness, which depends on the actual electric field. The higher the electric field the thinner the oxide layer for the maximum probability. The tunneling probability is higher for higher electric fields. These results indicate that the optimal charging behaviour of MNOS structures without nanocrystals can be expected for an oxide thickness of 2-3 nm.

The tunneling probability via the oxide layer (direct tunneling to NCS located at the SiO_2/Si_3N_4 interface) doesn't depend strongly on the electric field, but exhibits fast decrease with increasing the oxide thickness. For a given electric field the two extremes merge at a certain value of oxide thickness. So, the presence of nanocrystals enhances the electron injection at thin oxide layers only, and if NCs are located close to the SiO_2/Si_3N_4 interface (within the tunneling length).

Similar results were obtained for hole tunneling, but the maximum probabilities in MNOS structures without nanocrystals were obtained for thinner oxides about 1.5-2.5 nm.

Three simulated memory hysteresis curves are presented in Fig. 3 that demonstrate the effect of existence of nanocrysals at the SiO_2/Si_3N_4 interface. One curve is calculated for a structure without NCs, the others for a structure containing Si NCs with a size of 3 nm. Tunneling via the NCs to a depth of 6 nm or direct tunneling to NCs and capture by them are considered.

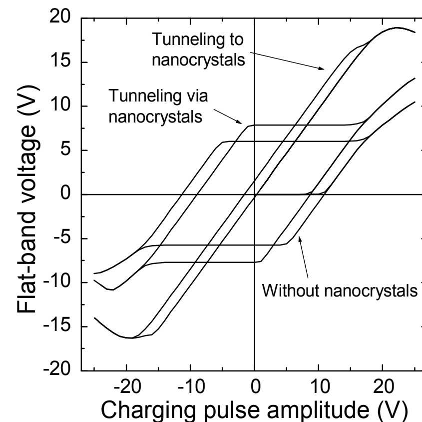

Figure 3. Simulated memory hysteresis curves exhibiting the effect of presence of nanocrystals located at the SiO_2/Si3N_4 interface. The oxide and nitride thicknesses are 2 nm and 30 nm, respectively, the depth of charge centroid is 6 nm, nanocrystal size is 3 nm, the pulse width is 10 ms.

The hysteresis loops can be characterized by their height and width. The height is connected to the maximum charge that can be injected and stored in the structure, while the width is related to the electric field accuring in the oxide layer at the end of the charging pulse. It is seen in Fig. 3 that the memory hysteresis is thinner and higher for the structure containing NCs indicating enhanced charge injection and storage behaviour. But, the hysteresis loop is rather thin for direct tunneling to NCs. This is due to high tunneling probability and so high current level via the oxide layer. So, the system is closer to equilibrium, which can reached at higher current levels via the oxide layer. Such a situation is shown is Fig. 4, where the memory behaviour is collapsed for direct tunneling to NCs yielding a line with slope of unity instead of a hysteresis loop.

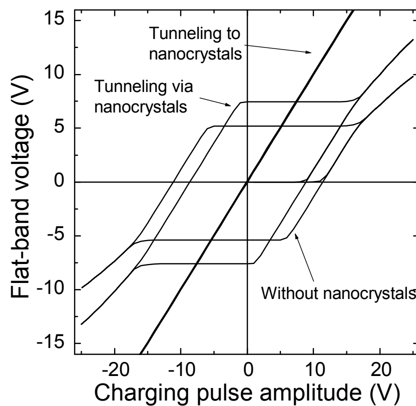

Figure 4. Simulated memory hysteresis curves exhibiting the collapse of memory behaviour at high tunneling probabilities (oxide currents). Nanocrystals are located at a depth of 1 nm. The oxide and nitride thicknesses are 1 nm and 30 nm, the depth of charge centroid is 6 nm, NC size is 3 nm, the pulse width is 10 ms.

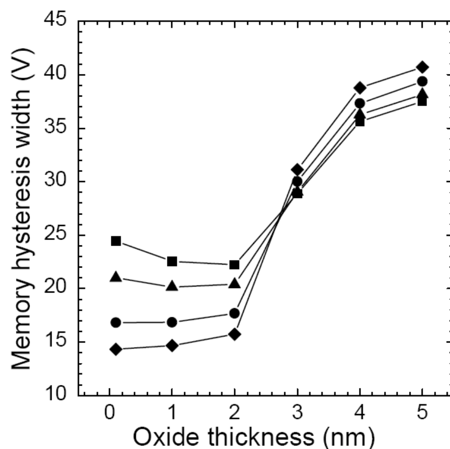

Figure 5. The width of memory hysteresis simulated for structures without (sqares) and with nanocrystals at the SiO_2/Si_3N_4 interface with nanocrystal layer thickness of 1 nm (triangles), 3 nm (circles) and 5 nm (diamonds).

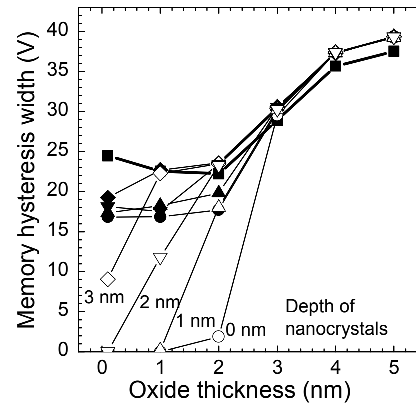

Figure 6. The width of memory hysteresis simulated for structures without (sqares) and with nanocrystals at a depth from the SiO_2/Si_3N_4 interface of 0 nm (circles), 1 nm (triangles up), 2 nm (triangles down) and 3 nm (diamonds). Open symbols are for direct tunneling to nanocrystals, solid symbols for tunneling via nanocrystals. The size of nanocrystals is 3 nm.

Fig. 5 presents the effect of the presence of NCs on the width of memory hysteresis as a function of oxide thickness for three different nanocrystal sizes. It is seen that NCs enhances the charging behaviour for thin oxide layers only below 3 nm, as it has been concluded on the basis of tunneling probabilities [4]. The larger the nanocrystals the higher their effect. The increasing width of the hysteresis above an oxide thickness of 3 nm is due to the voltage drop on NCs yielding lower electric field in the oxide layer for the same charging pulse amplitude.

Fig. 6 presents the width of memory hysteresis as a function of oxide thickness for different depth of nanocrystals from the SiO_2/Si_3N_4 interface. The effect of nanocrystals decreases with increasing depth.

IV. CONCLUSIONS

The effect of the oxide thickness and the depth, size and location of semiconductor nanocrystals has been studied on the charging behaviour of MNOS non-volatile memory structures by the calculation of electron and hole tunneling probability to the nanocrystals or to the nitride conduction or valence band, respectively, and by the simulation of memory hysteresis behaviour. The tunneling probabilities have been calculated by WKB approximation. The memory hysteresis behaviour were simulated by the integration of the difference of the current flowing into the structure via the tunnel oxide layer and that of flowing out of structure via the blocking layer, over the charging pulse width.

It has been obtained for MNOS structures that the tunnel oxide thickness, which is optimal for charge injection, is about 2 nm. The presence of nanocrystals enhances the charge injection resulting in better performance, but for structures with thin tunnel oxide layer (below 3 nm) only, and if the nanocrystals are located close to the oxide/nitride interface, i.e., when they are within the tunneling depth. But in the case of very high tunneling probability, i.e., of high tunneling currents the system approaches eqilibrium and the memory behaviour collapses.

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