Simulation of MNOS memory hysteresis - Effect of layer thicknesses

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Abstract— **MNOS memory hysteresis curves are simulated by integrating the difference of the current via the oxide and nitride layer. The effect of the oxide and nitride thickness as well as the depth of charge centeroid is studied. The results indicate that the optimal oxide thickness is about 2 nm. A thin nitride layer decreases the efficiency of the injected charge. It has been obtained that the possible highest memory window width decreases monotonically with increasing depth of charge centroid.**

I. INTRODUCTION

The two basic types of memory elements used in non-volatile (EEPROM and flash) memories are the floating gate and the SONOS (silicon-oxide-nitride-oxide-silicon) field effect transistors (FETs). Floating gate memory arrays face difficulties with technology scale-down. The main problem is that through defects or weak points of tunnel oxide with reduced thickness the whole amount of stored charge carrying the information can be lost. One of the possible solutions is to replace floating gate with separated semiconductor nanocrystals, which are electrically isolated [1-10].

But, in SONOS and MNOS (metal-nitride-oxide-silicon) devices (the latter were the first realized memory structures [11]) the charge is stored in traps located in the Si_3N_4 layer close to the Si_3N_4/SiO_2 interface. In these structures traps are isolated a'priori [8-10]. Therefore, these structures are more scalable without using nanocrystals. However, as the reduction of lateral dimensions involves the reduction of layer thicknesses as well, the study of their effect on the memory behaviour is important and topical.

One of the characteristic features of MNOS memory structures is the hysteresis of the threshold voltage of field effect transistors or of the flat-band voltage of capacitors on the amplitude of charging voltage pulses [11-15]. In this work memory hysteresis curves obtained by computer simulation are presented. The effect of the layer thicknesses, namely of the oxide and nitride thickness and of the depth of the injected charge centroid on the hysteresis behaviour have been studied.

A part of the obtained results is applicable for SONOS structures as well, because the main difference between the memory behaviour of MNOS and SONOS structures is the reduction of current level via the control layer by an additional oxide layer on the top of the structure.

II. SIMULATION DETAILS

The charge injected via the thin oxide layer is captured and stored in traps in the nitride layer close to the oxide/nitride interface. The net charge captured in the nitride layer during a voltage pulse can be calculated by the integration of the difference of the current flowing into the structure via the oxide layer and that of flowing out of structure via the nitride layer, over the charging pulse width τ [11]:

$$\Delta\sigma_3 = \int_0^{\tau} (J_{ox} - J_n)dt \quad (1)$$

The oxide current can be expressed as [12]:

$$J_{ox} = C_{FN} E_{ox}^2 P \quad (2)$$

where C_{FN} is a constant, E_{ox} the electric field in the oxide and P the tunneling probability via the potential barrier, which can be expressed as [16]:

$$P = \exp\left(-\frac{2}{\hbar} \int_{x_1}^{x_2} \sqrt{2m^*[U(x) - E]}dx \right) \quad (3)$$

Here x_1 and x_2 are the coordinates, where the electron enters and leaves the potential barrier (turning points), m^* is the effective mass of the electron, $\hbar$ is the Planck constant (devided by 2π), $U(x)$ is the potential energy as a function of coordinate, and E is the electron energy.

The current via the nitride layer has been obtained by experiment [17]:

$$J_n = J_{PF} + J_{EX} \quad (4)$$

where JPF is the Poole-Frenkel current:

$$J_{PF} = C_{PF1} \cdot E_n \cdot \exp\left(C_{PF2} \cdot \sqrt{E}_{n2}\right) \quad (5)$$

(here C_{PF1} and C_{PF2} are parameters depending on the insulator properties and E_{n2} is the electric field in the nitride layer between the charge centroid and the metal) and J_{EX} is an excess current obtained at low voltages [17]:

$$J_{EX} = C_{EX1} \cdot \exp(C_{EX2} \cdot E_{n2}) \quad (6)$$

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where C_{EX1} and C_{EX2} are parameters depending on the insulator properties.

The relation between the charging voltage amplitude and the oxide and nitride electric fields can be expressed as

$$V_P = E_{ox}d_{ox} + E_{n1}d_{n1} + E_{n2}d_{n2} \tag{7}$$

where d_{ox} is the oxide thickness and d_{n1} is the depth of charge centroid from the oxide/nitride interface. The relations between the electric fields can be obtained by the Gauss law:

$$\varepsilon_{ox}E_{ox} = \varepsilon_n E_n \tag{8}$$

$$\varepsilon_n E_{n1} = \varepsilon_n E_{n2} + \sigma_3 \tag{9}$$

where ε_{ox} and ε_n are the oxide and nitride permittivities. Finally, the flat-band voltage can be calculated via the charge in the nitride layer as

$$V_{FB} = -\frac{\sigma_3}{\varepsilon_n} d_{n2} \tag{10}$$

The integration has been performed for each charging pulse amplitude by Eqs. (1-10). The actual barrier height values and C_{FN} have been taken from Ref. [12], while the parameters for the nitride current from Ref. [17]. The hysteresis curves were begun to be calculated from zero pulse amplitude and zero flat-band voltage. The voltage pulse amplitude was increased or decreased by 1 V step by step. The effect of oxide thickness has been studied in the range of 1-10 nm for structures with a total thickness of nitride layer of 30 nm and with constant depth of charge centroid of 6 nm. The effect of nitride thickness has been studied in the range of 10-40 nm for structures with d_{ox}=2 nm.

Two different cases were studied. In one case the charge cetroid was located at a fixed distance of 6 nm from the oxide/nitride interface, in the other case it was located at the 1/5 part of the total nitride thickness. The pulse width used for simulation was 10 ms.

III. Results and Discussion

Fig. 1. presents simulated hysteresis curves as a function of oxide thickness. The hysteresis curves can be characterized with two main parameters. The horizontal width (devided by 2) indicates the avarage pulse amplitude necessary for recharging the structure at the given pulse width. The vertical width of the hysteresis is connected to the highest amount of charge that can be stored in the structure. It determines the highest width of the memory window for the given structure and pulse width.

Increasing the oxide thickness from 1 nm to 2 nm, the obtained hysteresis curve indicates increasing highest amount of charge in the structure for a little lower charging voltages. But increasing the oxide thickness further, the amount of possible stored charge decreases fast, while the pulse amplitude necessary for recharging increases. From 4 nm up to 10 nm the highest possible amount of charge does not change further, while the pulse amplitude increases slowly. It is connected to the change of charge injection mechanism from direct to Fowler-Nordheim tunneling.

These results are in agreement with the results of our earlier calculations [16]. Studying the effect of oxide thickness on the tunnelling probability at different electric fields it was concluded that the optimal oxide thickness is 2-3 nm [16]. The simulation of hysterezis curves indicates an optimal oxide thickness about 2 nm.

The results obtained here are in agreement with our experimental results as well, which were obtained in MNOS structures with and without Si [8] or Ge nanocrystals [9,10]. MNOS structures with different oxide thicknesses were studied, and the best charging behaviour were obtained for an oxide thickness of about 2 nm.

The effect of nitride thickness can be seen in Figs. 2 and 3. Fig. 2 presents the hysteresis curves obtained for the case when the charge centroid is a 1/5 part of the total nitride thickness, while hysteresis curves presented in Fig. 3 are obtained for a fixed charge centroid of 6 nm. In the first case the shape of hysteresis curves is similar, both the horizontal and vertical width decrease proportional to the decreasing nitride thickness. But in the case of a fixed depth of charge centroid the vertical width of the hysteresis decreases faster than the horizontal width. This case is closer to reality. So, in real cases the memory window shrinks faster with decreasing nitride thickness, than the charging pulse amplitude decreases. Therefore, a thin nitride layer decreases the efficiency of the injected charge. One should make a compromise between the low charging pulse amplitude and the memory window width.

The effect of the depth of charge centroid has also been studied. It was obtained that for the same voltage pulse amplitude the flat-band voltage decreases linearly with inreasing depth of charge centroid, as can be seen in Fig. 4. So, the possible memory window width decreases monotonically with increasing depth of charge centroid.

Therefore, for optimal charging behaviour the depth of injected charge centroid should be minimized. However, it is rather complicated to influence the depth of charge centroid by technology, on one hand. On the other hand, the retention time (the long of information storage) is better for deeper location of the injected charge [18]. So, if even one can influence the location of charge centroid, he has to make a compromise between the memory window width and retention time.

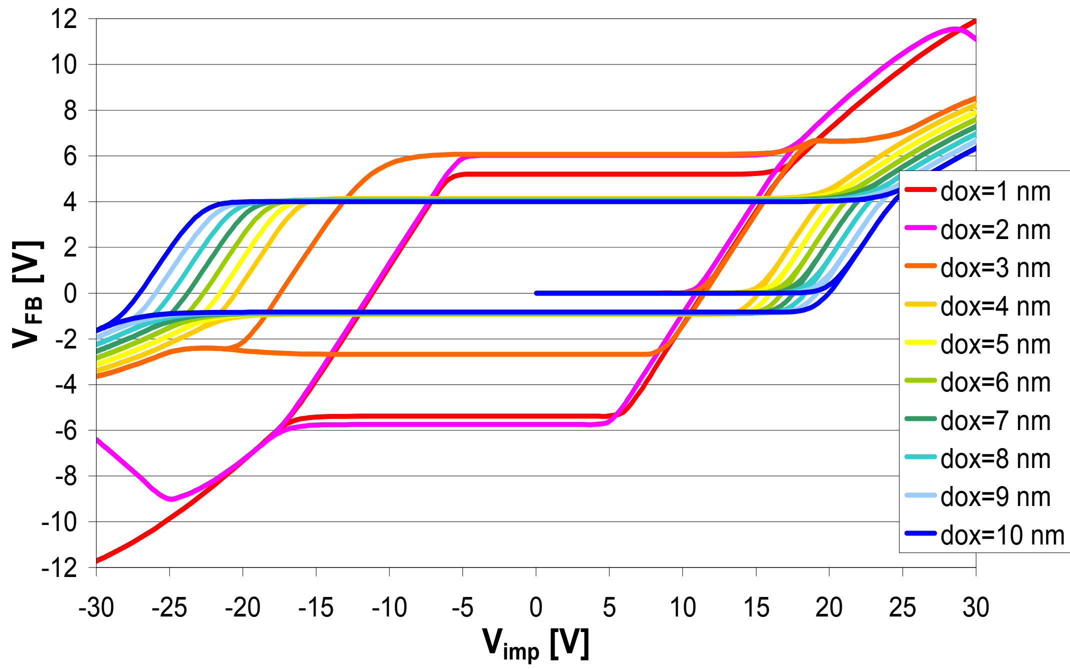

Figure 1. Simulated hysteresis curves as a function of oxide thickness in the range of 1-10 nm. The nitride thickness is 30 nm, the depth of charge centroid is 6 nm, the pulse width is 10 ms. The hysteresis curves are begun to be calculated from zero pulse amplitude and zero flat-band voltage. The voltage pulse amplitude is increased or decreased by 1 V step by step.

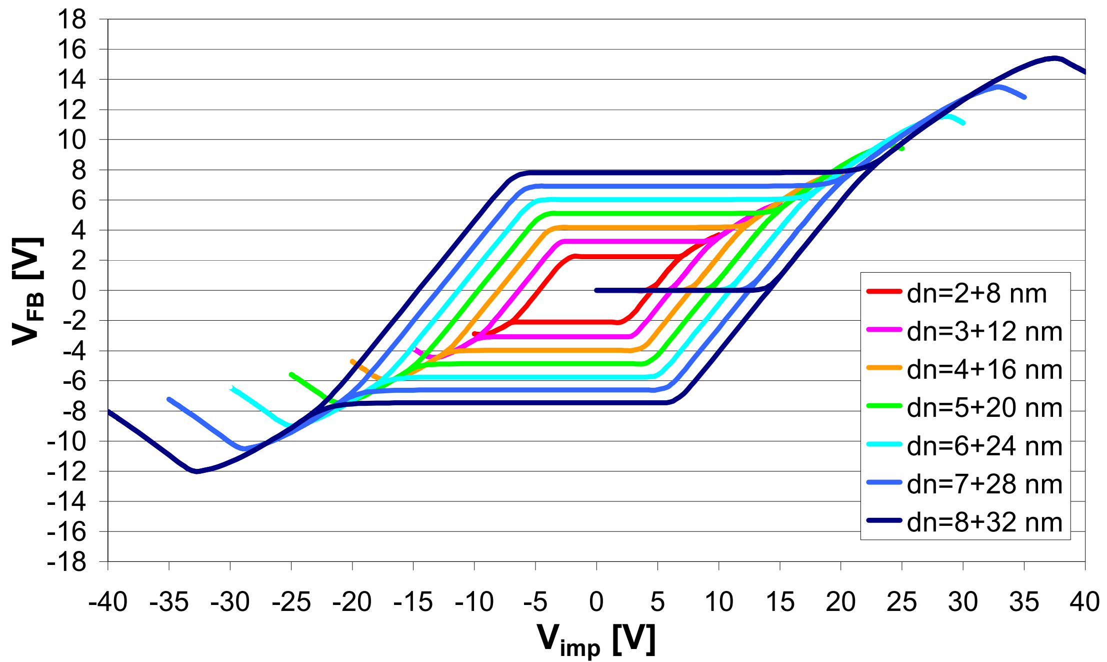

Figure 2. Simulated hysteresis curves as a function of nitride thickness in the range of 10-40 nm. The oxide thickness is 2 nm, the depth of charge centroid is 1/5 part of the total nitride thickness, the pulse width is 10 ms. The voltage pulse amplitude is increased or decreased by 1 V step by step.

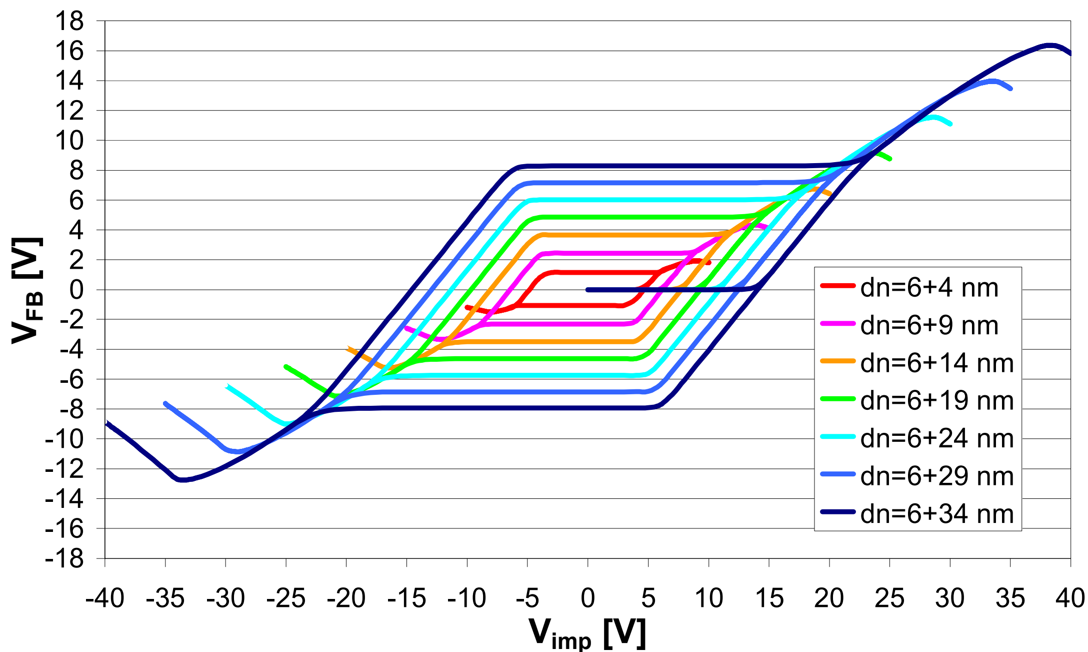

Figure 3. Simulated hysteresis curves as a function of nitride thickness in the range of 10-40 nm. The oxide thickness is 2 nm, the depth of charge centroid is 6 nm, the pulse width is 10 ms. The voltage pulse amplitude is increased or decreased by 1 V step by step.

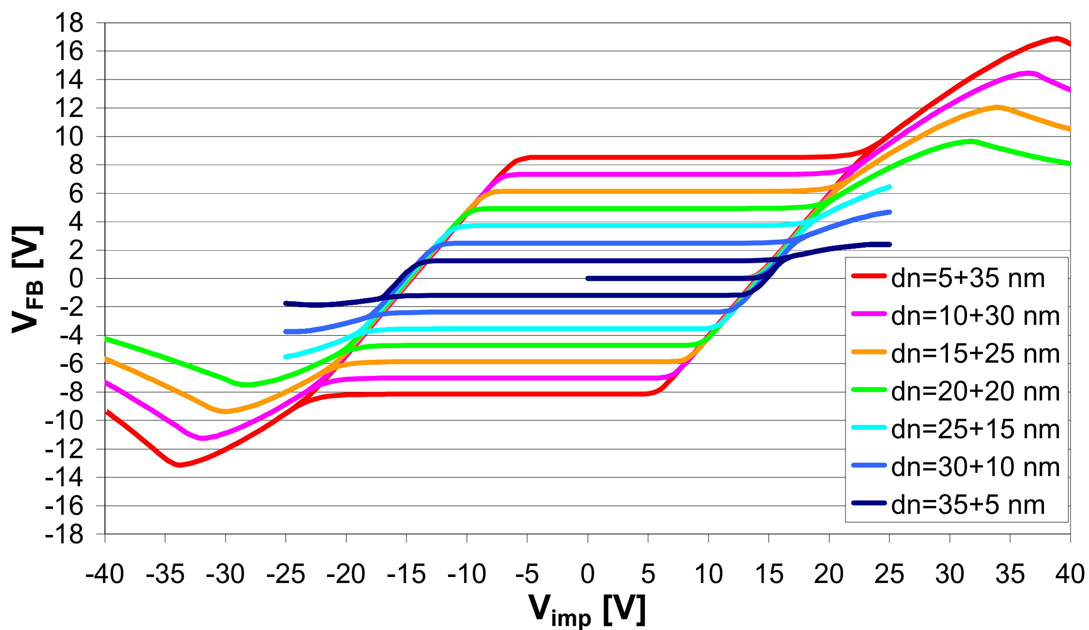

Figure 4. Simulated hysteresis curves as a function of depth of charge centroid from the oxide/nitride interface in the range of 5-35 nm. The oxide thickness is 2 nm, the nitride thickness is 30 nm, the pulse width is 10 ms. The voltage pulse amplitude is increased or decreased by 1 V step by step.

IV. Conclusions

MNOS memory hysteresis curves have been calculated. The effect of the oxide and nitride thickness as well as the depth of charge centroid has been studied. It has been concluded that the optimal oxide thickness is about 2 nm, in agreement with experimental results. The decrease of nitride thickness decreases the efficiency of the injected charge. Choosing the nitride thickness one makes a compromise between the low charging pulse amplitude and the memory window width. It has also been obtained that the possible highest memory window width decreases monotonically with increasing depth of charge centroid.

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