Development of Complex Curricula for Molecular Bionics and Infobionics Programs within a consortial* framework**

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**Molekuláris bionika és Infobionika Szakok tananyagának komplex fejlesztése konzorciumi keretben

***A projekt az Európai Unió támogatásával, az Európai Szociális Alap társfinanszírozásával valósul meg.

VLSI Design Methodologies

(VLSI tervezési módszerek)

Introduction to Manufacturing of Integrated Circuits

(Bevezetés a Integrált Áramkörök Gyártásába)

PÉTER FÖLDESY

This course gives an introduction to integrated circuits.

Starting from its raw materials, manufacturing process through the low level design issues up to the system level conserns.

The key competences of this course are the wide view of this complex technology, economical aspects, practical experiences of the advanced CAD tools.

The topics of this course:

- Trends in IC design
- Manufacturing process
- Building blocks of Integrated Circuits
- Connection between designed and manufactured structures
- Digital and analog design flows
- Low-power design
- Image, MEMS sensors and their design
- 3D integration technologies, why and how

The topics are covered in this chapter:

- Overview of IC design
- Technology roadmap and trends
    - Motivations behind and consequences
- Basic materials, methods and measures
- Manufacturing process and relation to design methods and CAD tools

Section I

The wide overview of integrated circuit design and manufacturing

Integrated circuit designs are classified as:

- Analog
  - Small transistor count precision circuits such as Data converters, Sensors etc.
- *Application Specific Integrated Circuits - ASICs*
  - These are IC's that are created for specific purposes. The most common application area for this is DSP - signal filters, image compression.
- SoC or Systems on a chip:
  - These are highly complex circuits. A network processor chip or a wireless radio chip is an example of an SoC.

How the ICs are designed?

- At low level, basically using polygon drawing tools to draw each mask. Polygons are translated to photolithograpy driven manufacturing steps.
- At higher level, automated CAD tools synthesizes the textual hardware description to cell and IP block seas.
- At the top, only hard IPs are wired together, and mostly software engineering remains.

While digital design is highly automated – but not a trivial task, small portion of analog design covered by automated tools.

There is no generic analog description language, as behavioral models cannot capture the complexity of the effects of parasitic on the analog behavior of the circuit.

For more complex analog chips such as data converters, the design is done at a transistor level, building up to a module level, then a block level and then integrated at a chip level. Analog design remains a difficult art.

Overview of manufacturing costs, methods

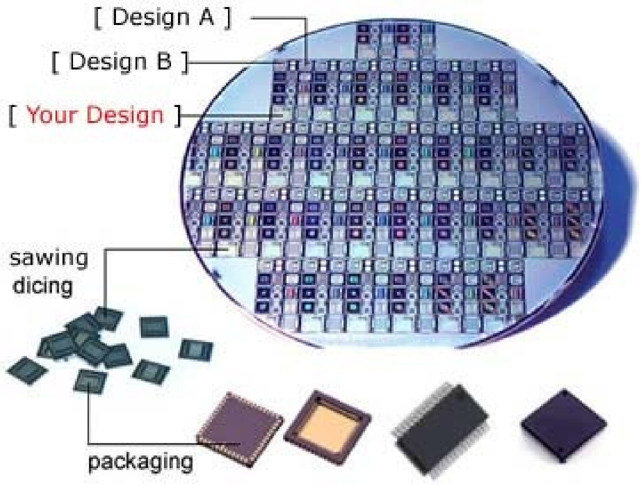
- Worth to create dedicated integrated circuit if
  - Unique physical role (sensor, shape for neuroprobe)
  - >100k pieces are needed
  - Learning curve
- Costs, just manufacturing
  - Above 180 nm node, ~50-100k$
  - Below 45 nm node, million $ for mask generation only

Overview of manufacturing costs, methods

- Cost sharing for prototyping: multi-project wafers
- In order to make the technology better, the complexity and cost rises exponentially. So, less and less fabs are in the worlds
  - ~1 um CMOS worked in Hungary and now advanced MEMS laboratory operates in MTA-MFA
- The common IC manufacturing is done far from the factories. These design companies are called *Fabless Design House*.

MPW offering agencies:

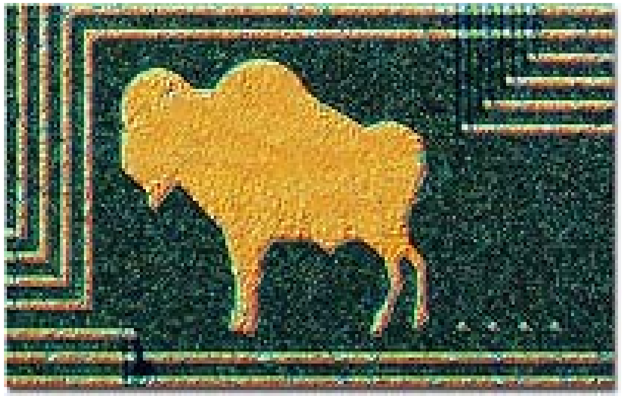
Name	*Region, funding*
Europractice	Belgium, partially supported, largest
MOSIS	USA, not supported, self-cost
CMP	France, but, accessible in EU
CIC	Taiwan, fully paid, but for the country
VCEC	Japan
IDEC	Korea
ICC	China
CMC	Canada
FUMEC	Mexico

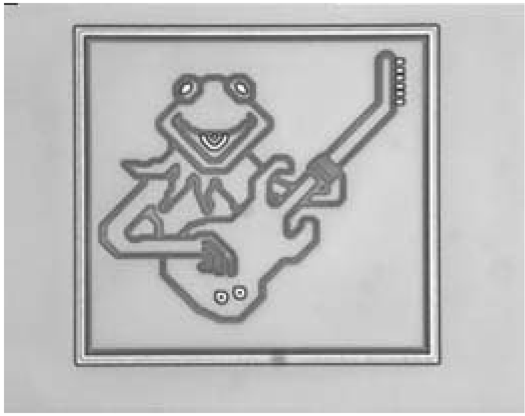


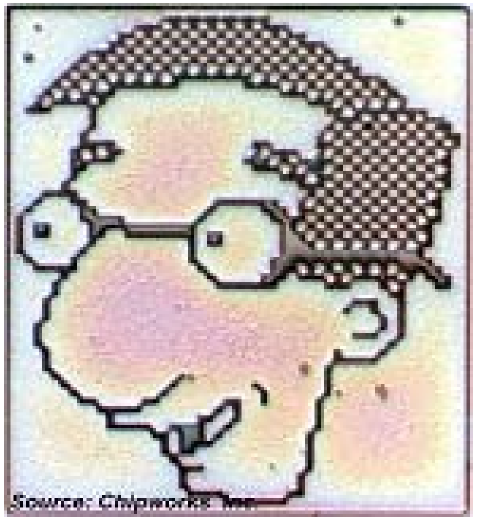
Europractice flyer

Silicon can handle “art” as well (look for silicon zoo)

- In the area of hand crafted layouts, the art has been a common fun for designers
- Nowadays, the CAD tools does not allow too much special structures, they easily spot the art figures as errors, simply because they do not part of the circuitry.
  (and the worker is not paid for it).







Source: Chipworks Inc.

http://chipworks.com

Section II

Technology roadmap, scaling down and trends

Aspects of scaling

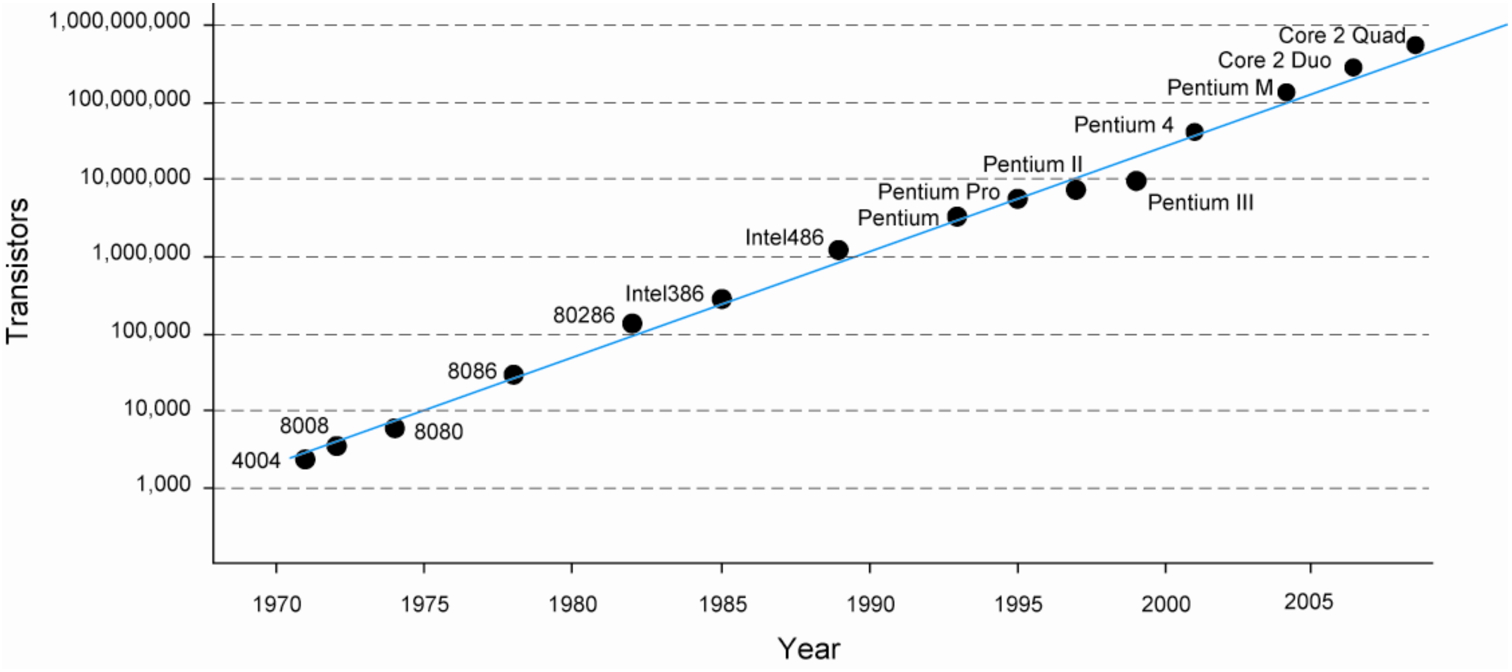
- Classic Scaling, just smaller (“More Moore”)
- Functional Diversification (“More than Moore”)
  - Integrated heterogeneous systems
- “Beyond CMOS” emerging research devices and materials, like
  - carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switches, and nano-electro-mechanical-system (NEMS) switches.

Scaling down (“More Moore”)

- Geometrical (constant field) Scaling—refers to the continued shrinking of horizontal and vertical physical feature sizes
- Non-geometrical process techniques and new materials that affect the electrical performance of the chip
- Design Equivalent Scaling
  - design-for-variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); heterogeneous multi-core SOC architectures

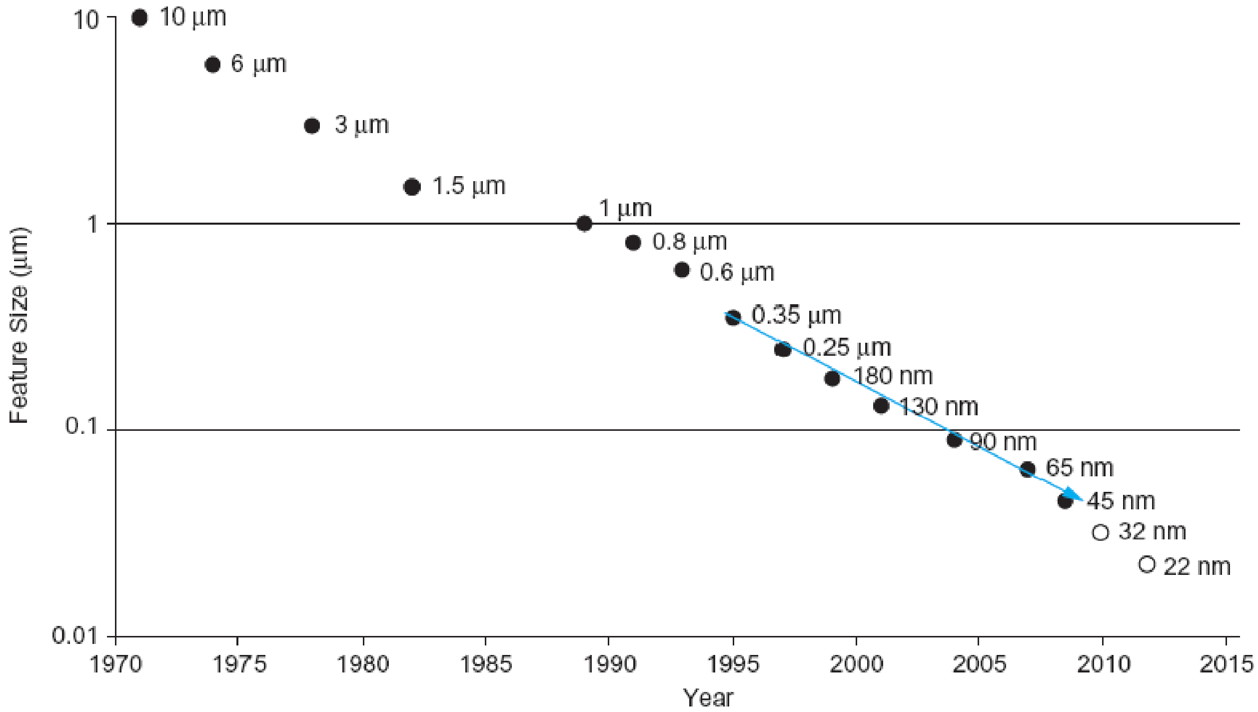
Scaling ("More Moore")

- Gordon Moore has identified in 1965 a trend of transistor counts (doubled every 26 months)



http://www.itrs.net/Links/2009ITRS/

- This trend is allowed by the smaller and smaller device and metalization size. When a design became larger than ~1 cm^2 (yield, packaging, productability limit) the next node came.



http://www.itrs.net/Links/2009ITRS

Functional Diversification (“More than Moore”)

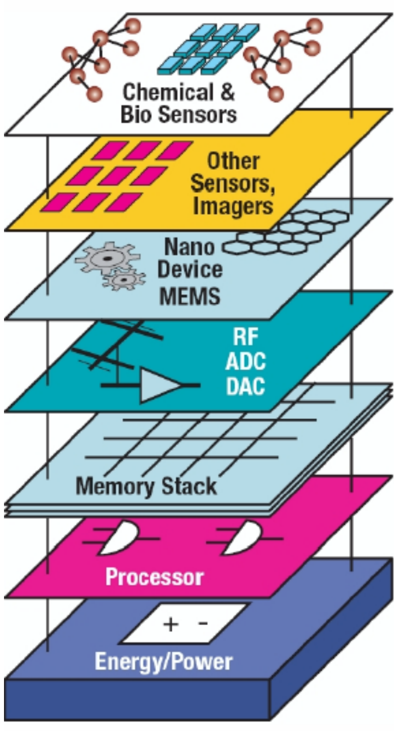
- Systems providing additional value to the end customer in different ways, e.g. non-digital functionalities like:
  - RF communication, power control, passive components, sensors, actuators
  - Migrating from the system board-level (PCB) into a particular package-level (SiP) or chip-level (SoC) solution.
- Novel technologies of 3D integration instead of planar

Application area specific technologies

- DRAM
- MPU/ASIC
  - Logic, analog, RF for wireless communication
  - High-voltage for display driver, LCD, OLED, MEMs driver
- Flash
  - NAND, NOR flash memories
- Various sensors (optical and other)
  - CCD and CMOS photosensors
  - Biochips, chemical detectors, actuators (CMOS+MEMS)

Advent of the 3D integration

- Limiting factor is the connection distance and technology incompatibility
- So, the motivation to go 3D is basically threefold:
  - Reach higher integration, higher performance
  - Integrate non compatible technologies like different semiconductor technologies
  - 3D integration would allow multicore processors and other high connectivity architectures to adopt topographic interconnection topologies



Methods of the 3D integration

- Monolithic – Electronic components and their connections (wiring) are built in layers on a single semiconductor wafer.
- Wafer-on-Wafer – Two or more semiconductor wafers are aligned, bonded, and diced into 3D ICs.
  Vertical connections are either built into the wafers before bonding or else created in the stack after bonding. The via are called through-silicon via (TSV).
- Die-on-Wafer or Die-on-Die – A wafer is diced and piece-by-piece integrated on top of a complete wafer. The connection is may be wire bonding or flip chip.

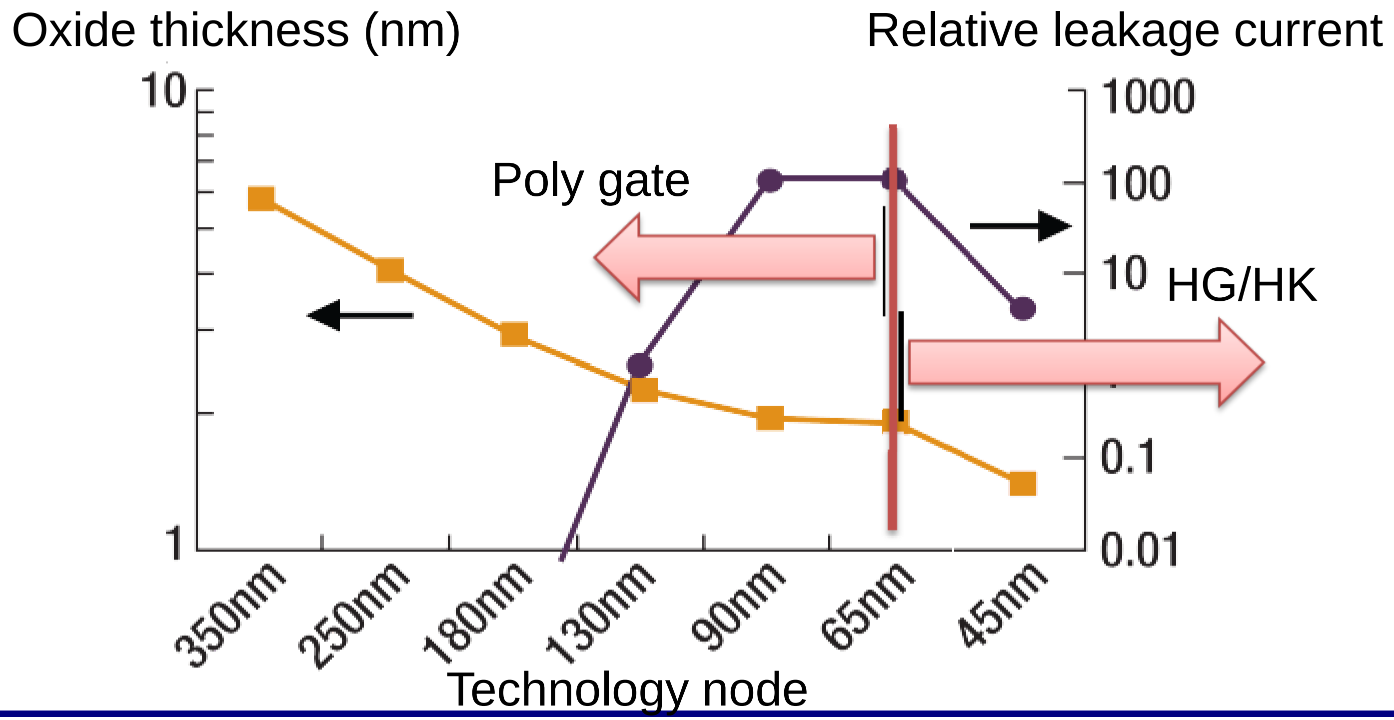
Consequences of size reduction (“scaling down”)

- Behavioral changes
  - Electrical behavior differs from classical models
  - Large leakage current, need for power management
- Technological
  - *Lithography* becomes non-trivial well below the wavelength (e.g. 193 nm UV light for 22 nm lines).
  - Application area specific technologies and materials
  - Usage of exotic materials
  - Cost of fabrication facilities increases
  - Complex gates are groups of atoms, not transistors

Electrical, behavioral changes

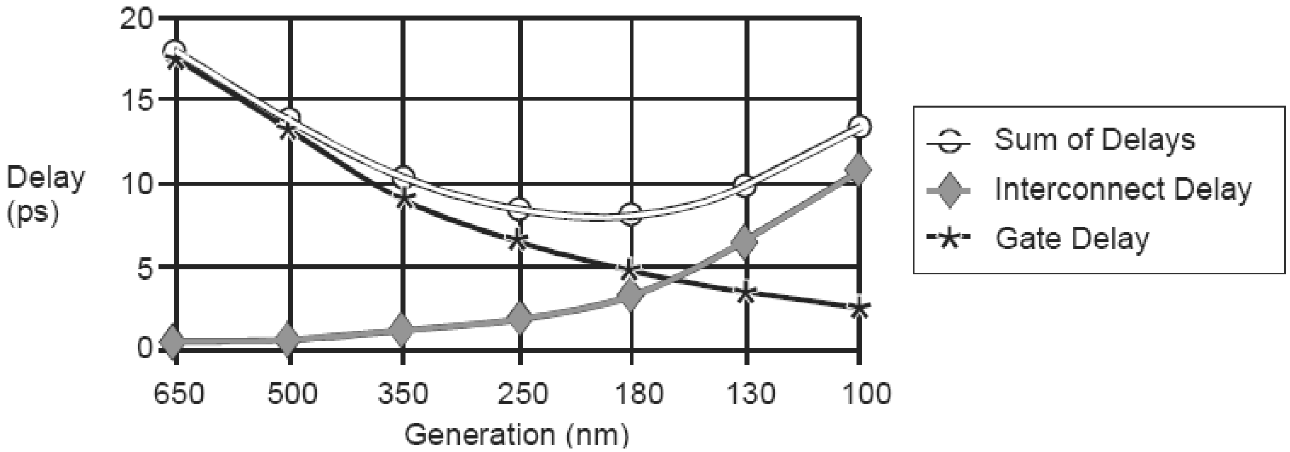
- Off state switches do not mean no current
  - High leakage current, both in channel and through gate oxide tunneling
  - Solution is thick gate oxide, “high-K” to replace SiO2 as the gate dielectric (at 90 nm node, the gate oxide is 1.2 nm – four atoms).
  - New oxide required new gate material instead of poly-Si
- Low voltage operation, no room for analog design
  - Power supply is in the range of 1V.

- To mitigate high leakage current, migrating from Poly/SiON to metal gate/high-k (MG/HK) enabled the resumption of electrical oxide thickness scaling, while reducing gate leakage.



Electrical, behavioral changes

- Gate delay becomes smaller than wire delay
- Transistors continue to improve at smaller scales. The performance improvement gained in transistor scaling is insignificant compared to the degradation effects of interconnect scaling.



Section III

Materials and complexity measures

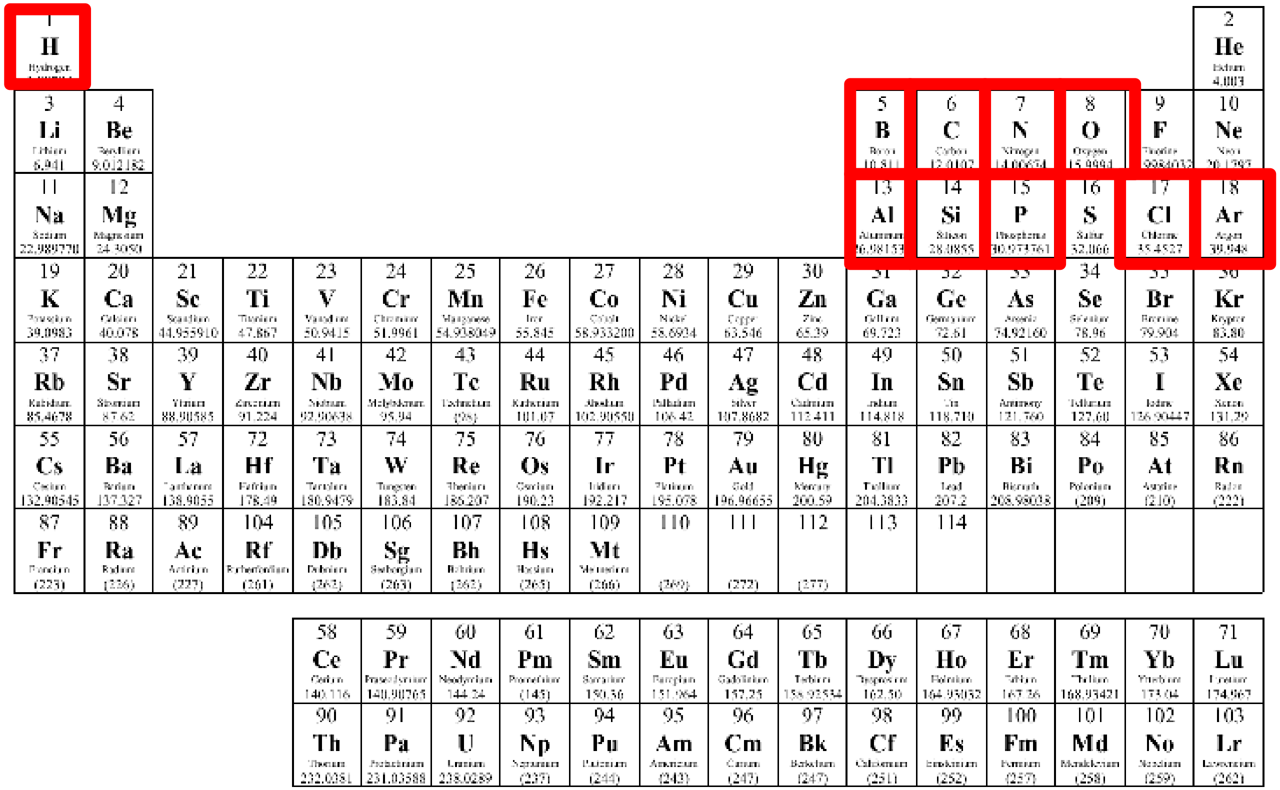
Overview of used raw materials.

- Substrate materials:
  - Semiconductors, because their conductivity, electrical properties can be locally controlled.
  - Silicon as material for wide-spread costumer electronics, in form of Silicon on Insulator (SOI) for high speed logic circuits, like processors.
  - Exotic materials, like GaAs for high frequency RF technologies, receivers, transmitters.
  - GaAlAs, InP, Mn doping for LEDs, solar cells

- Metals for electrical interconnection:
  - Aluminium, Copper for wiring
  - Tungsten for vias between wires
  - Gold for connecting integrated circuits to package
  - Hafnium, Rubidium, Tallium as metal gate of transistors
  - Indium for connecting integrated circuits to boards in flip-chip packages

- Other various materials:
  - Dopants to modify semiconductors (Phosphorus, Boron)
  - Silicon oxide, silicon nitrides for separation of conducting layers, wires, gates, substrate from each other.
  - Helper materials for aligning and matching crystal structure, like Titan.
  - Process materials, like Fluor as HF for semiconductor etching

Here we can see the materials involved in IC manufacturing as the time elapses in the periodic table.



1 H																	2 He
3 Li	4 Be											5 B	6 C	7 N	8 O	9 F	10 Ne
11 Na	12 Mg											13 Al	14 Si	15 P	16 S	17 Cl	18 Ar
19 K	20 Ca	21 Sc	22 Ti	23 V	24 Cr	25 Mn	26 Fe	27 Co	28 Ni	29 Cu	30 Zn	31 Ga	32 Ge	33 As	34 Se	35 Br	36 Kr
37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
55 Cs	56 Ba	57 La	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
87 Fr	88 Ra	89 Ac	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110 (269)	111 (272)	112 (277)	113	114				
				58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
				90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

1980's

VLSI Design Methodologies:
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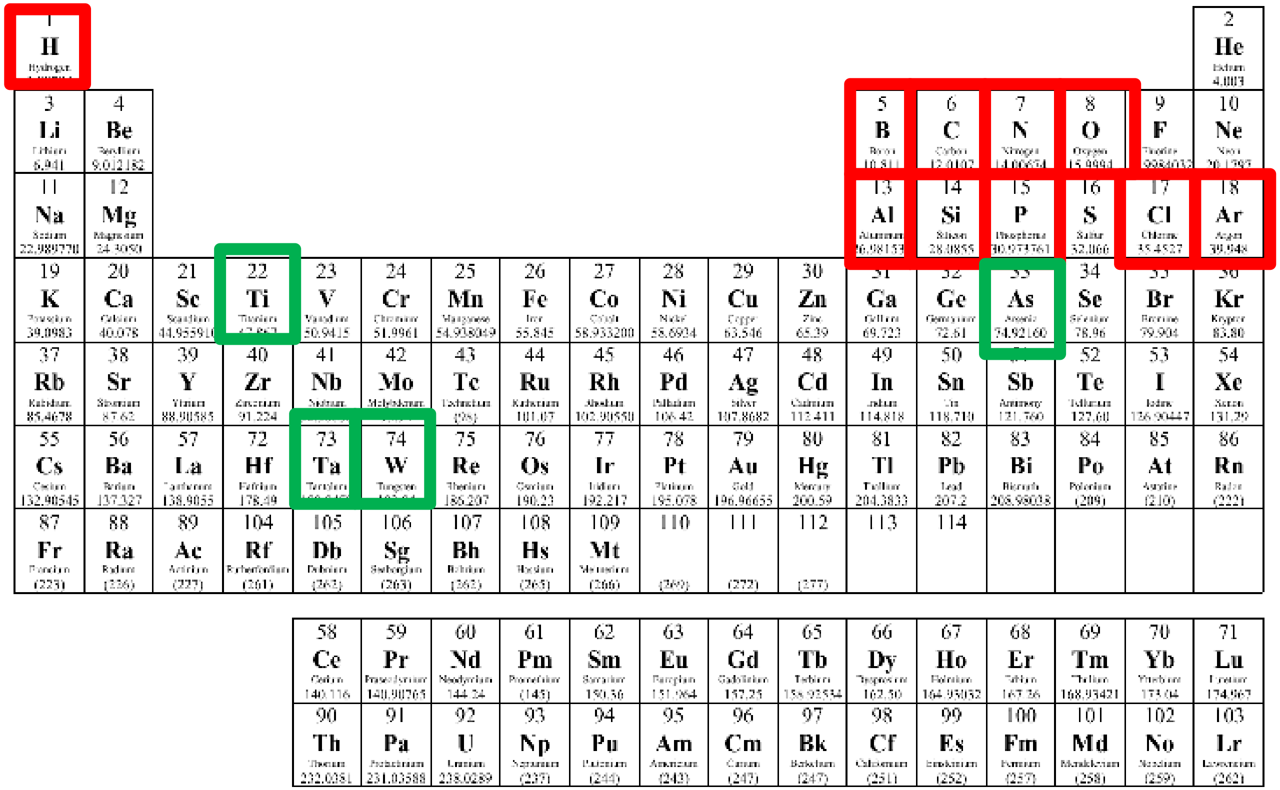

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37 Rb	38 Sr	39 Y	40 Zr	41 Nb	42 Mo	43 Tc	44 Ru	45 Rh	46 Pd	47 Ag	48 Cd	49 In	50 Sn	51 Sb	52 Te	53 I	54 Xe
55 Cs	56 Ba	57 La	72 Hf	73 Ta	74 W	75 Re	76 Os	77 Ir	78 Pt	79 Au	80 Hg	81 Tl	82 Pb	83 Bi	84 Po	85 At	86 Rn
87 Fr	88 Ra	89 Ac	104 Rf	105 Db	106 Sg	107 Bh	108 Hs	109 Mt	110	111	112	113	114				

58 Ce	59 Pr	60 Nd	61 Pm	62 Sm	63 Eu	64 Gd	65 Tb	66 Dy	67 Ho	68 Er	69 Tm	70 Yb	71 Lu
90 Th	91 Pa	92 U	93 Np	94 Pu	95 Am	96 Cm	97 Bk	98 Cf	99 Es	100 Fm	101 Md	102 No	103 Lr

1990’s

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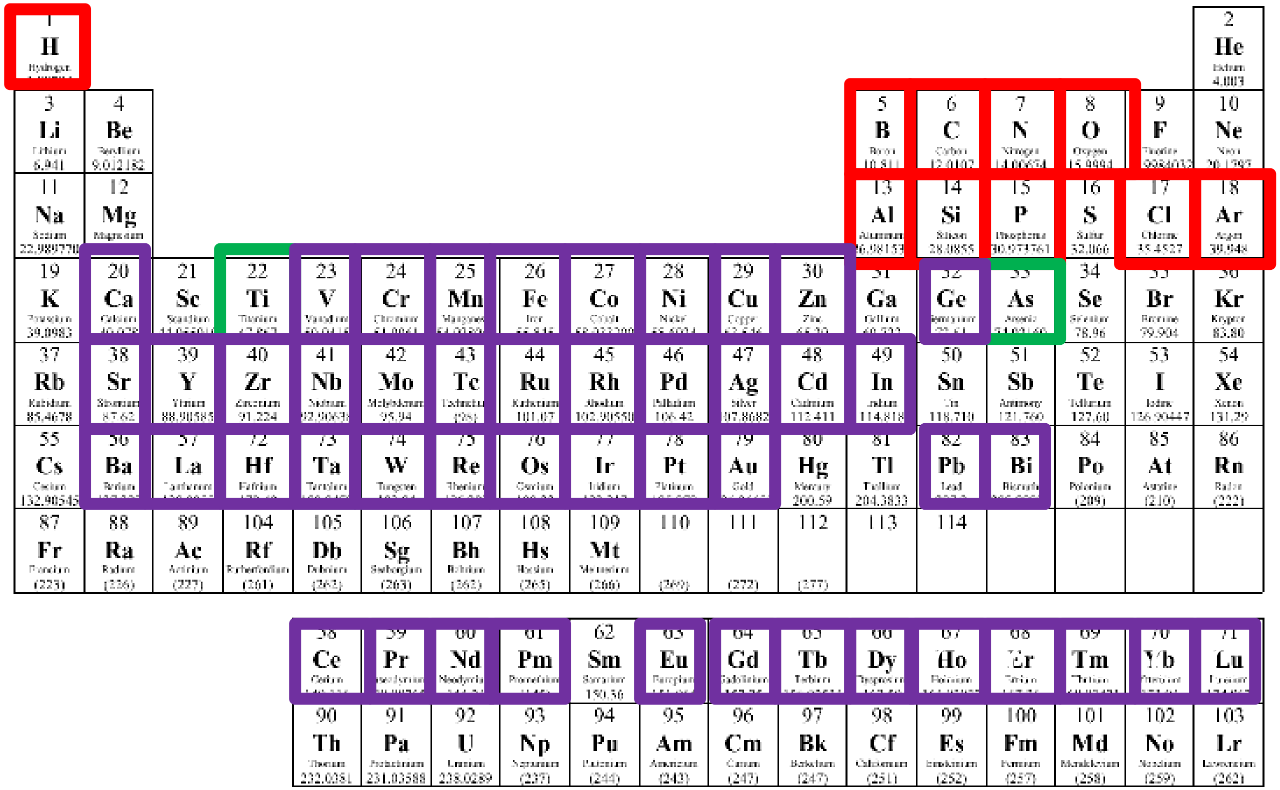
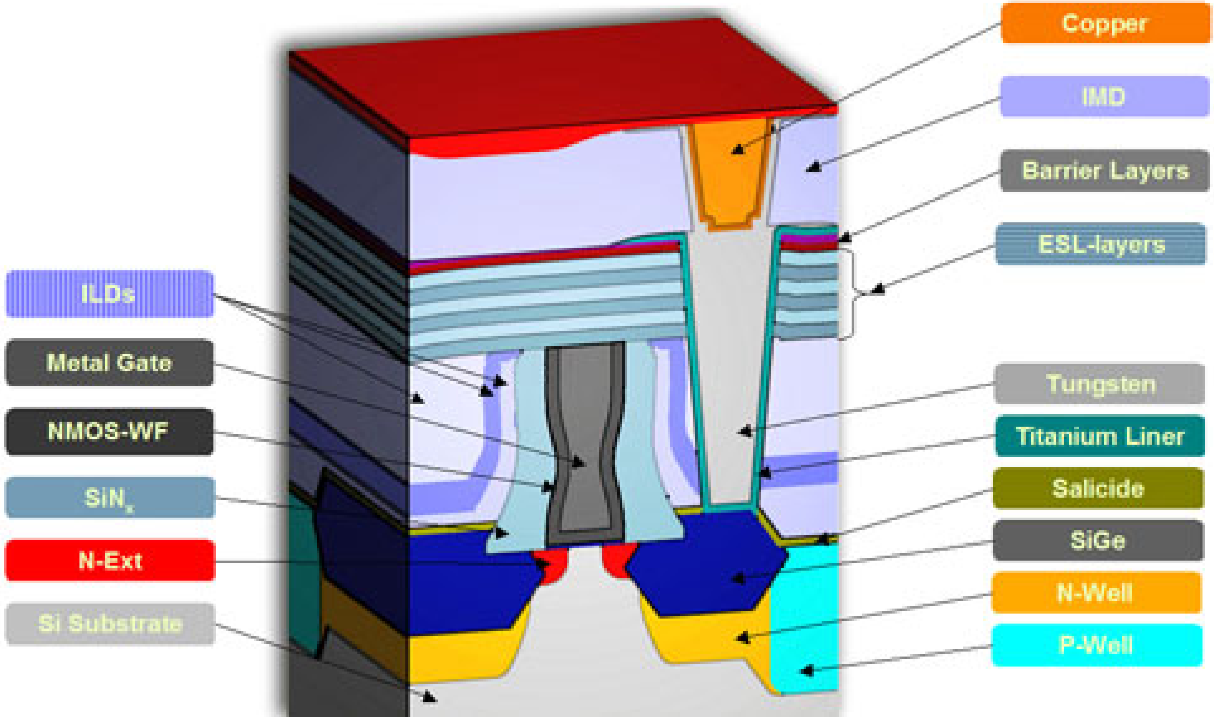


2000’s



22 nm metal gate transistor cross section. Note, that most of the materials are used to avoid diffusion of other structural blocks

Complexity measures

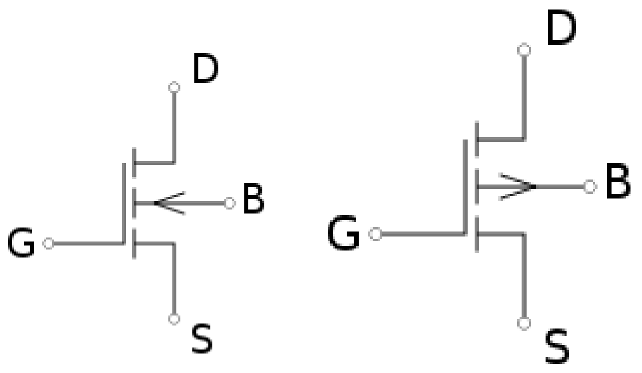
- SSI, MSI, LSI (small-, medium-, large-*scale integration*) under 100,000 transistors
- Over 100,000 transistors: VLSI (very large SI)
- More than 1 million: ULSI (ultra large SI)
- WSI (wafer-scale integration)
- SOC, system-on-a-chip, complex computers are integrated (analog front-end, memory, peripheries, processors)
- *Multi-chip-modules* and 3D technologies

What are the elements typically needed?

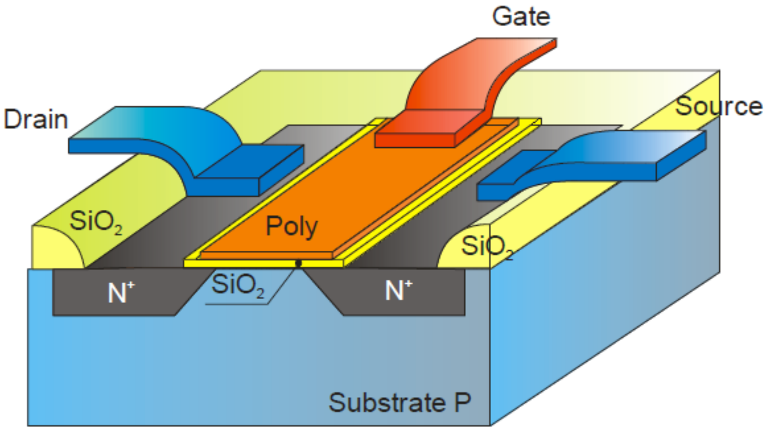
- Binary switch
- Analog controlled sources (current, voltage)
- Resistors
  - Doped diffusion, poly-Si
- Capacitors
  - Metal to metal wires, metal-insulator-metal (MIM)
  - Poly-Si to poly-Si
- Inductivity
  - Metal loops

MOS Transistor as well

MOS Transistor based elements



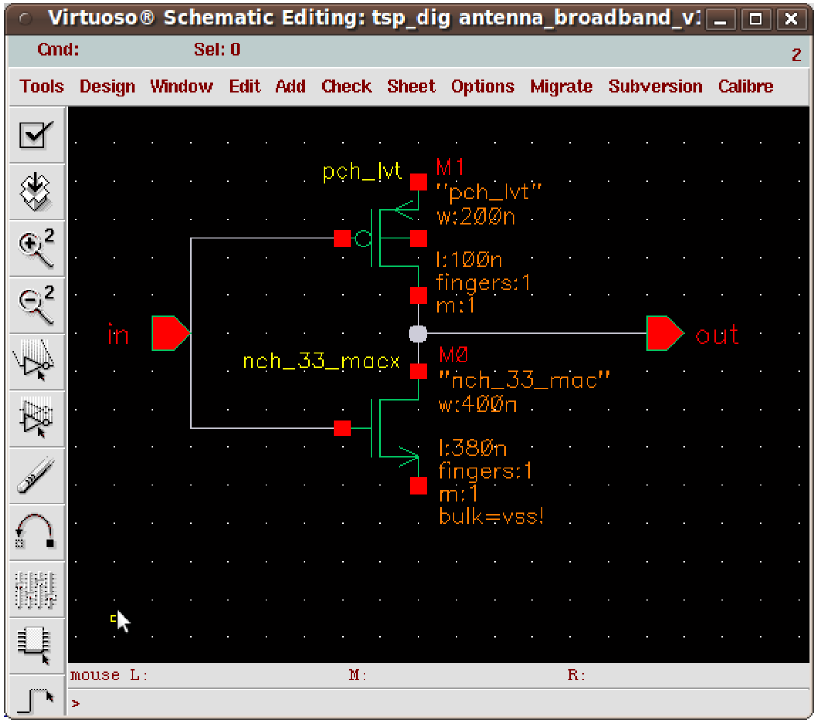
The symbol of the MOST



Rough cross section and bird's eye view

http://commons.wikimedia.org/wiki/File:MOSFET_Manufacture_-_7_-_metalisation.svg

MOS Transistor in the design environment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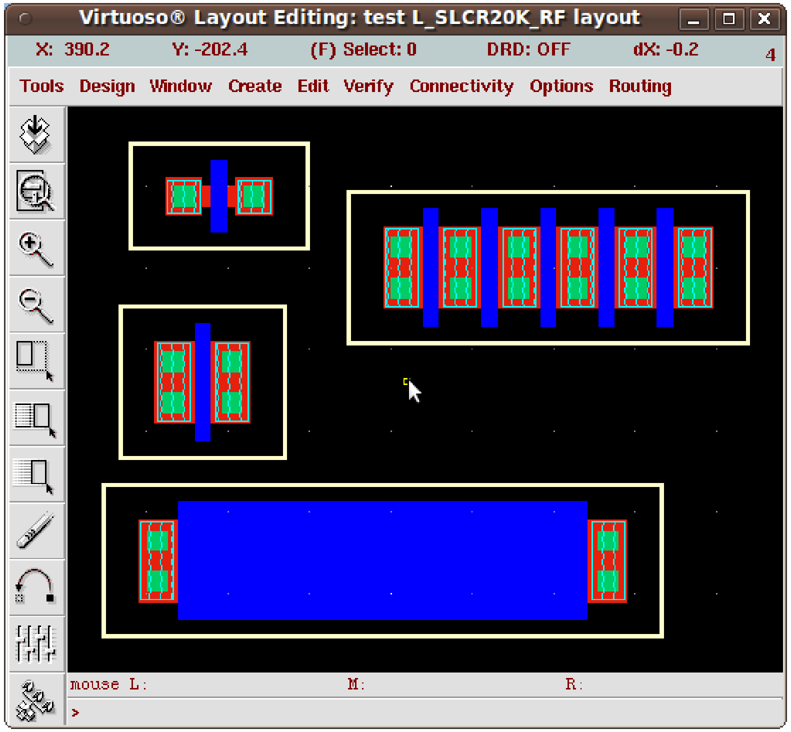
Schematic of two MOSTs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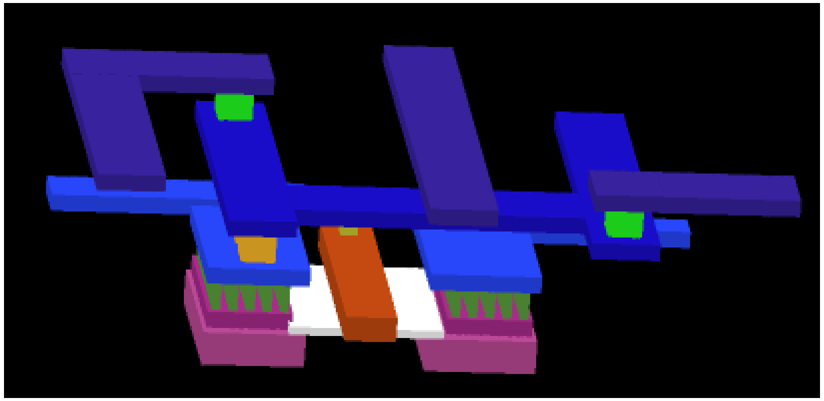
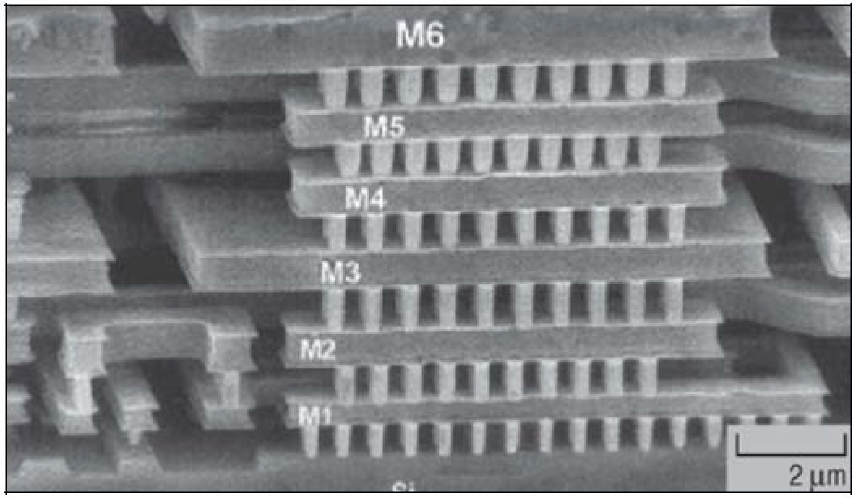
Layout of some MOSTs

Other views of the same transistors, circuits.



3D view of a MOST and its wiring

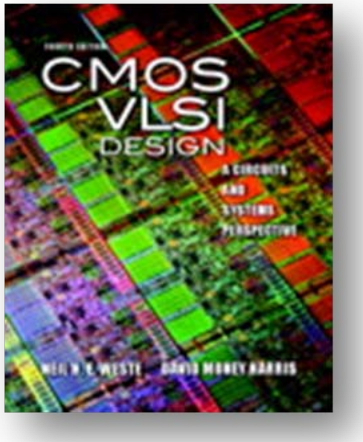


Final view of a 0.35 um technology with six metal layers.

Conclusions:

- We learned that the IC manufacturing is a difficult and expensive industry and business.
- There are a huge number of variants and technologies, there is no one and only method that fit all requirements.
- Fabless IC design is introduced and the design can be “anywhere”.

Recommended literature:



CMOS VLSI Design: A Circuits and Systems Perspective, 4/E
Neil Weste, *Macquarie University and The University of Adelaide*
David Harris, *Harvey Mudd College*
Publisher: Addison-Wesley

CMOS Transistor Layout KungFu ebook
Lee Eng Han et al.
www.eda-utilities.com/CMOS_Transistor_Layout_KungFu.pdf

Comprehension questions:

I. Which kind of trends exists in the integrated circuit industry?
II. What are motivations behind 3D integration?
III. What are the major classes of ICs?
IV. What does VLSI means?