Development of Complex Curricula for Molecular Bionics and Infobionics Programs within a consortial* framework**

Consortium leader

PETER PAZMANY CATHOLIC UNIVERSITY

Consortium members

SEMMELWEIS UNIVERSITY, DIALOG CAMPUS PUBLISHER

The Project has been realised with the support of the European Union and has been co-financed by the European Social Fund ***

**Molekuláris bionika és Infobionika Szakok tananyagának komplex fejlesztése konzorciumi keretben

***A projekt az Európai Unió támogatásával, az Európai Szociális Alap társfinanszírozásával valósul meg.

VLSI Design Methodologies

(VLSI tervezési módszerek)

Building blocks of Integrated Circuits

(Bevezetés a Integrált Áramkörök Gyártásába)

PÉTER FÖLDESY

The topics are covered in this chapter:

- Active elements and connection in between
- Analog blocks:
  - Actives, like *MOSFET* and derivatives
  - Passives, like capacitors, inductivity
- Digital blocks:
  - Random logics
  - *IP* blocks and their role
  - Design-reuse

Active elements and connection

- All CAD methodology is about blocks and connectors
- The reason is simple: this is the basis of modularity, design reuse, and constructive thinking and learning
- All the blocks are working at the same time (not a serial processor executed procedural program)
- In principle, the signaling does not alter other connections (no cross-talk)
  - If so, the tools and the methods strengthen the elements to suppress any cross-talk

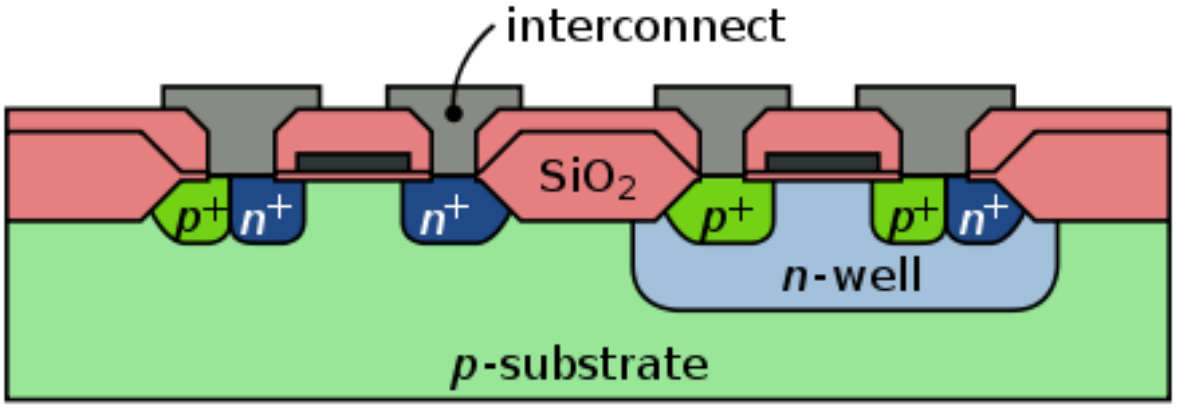
Section I

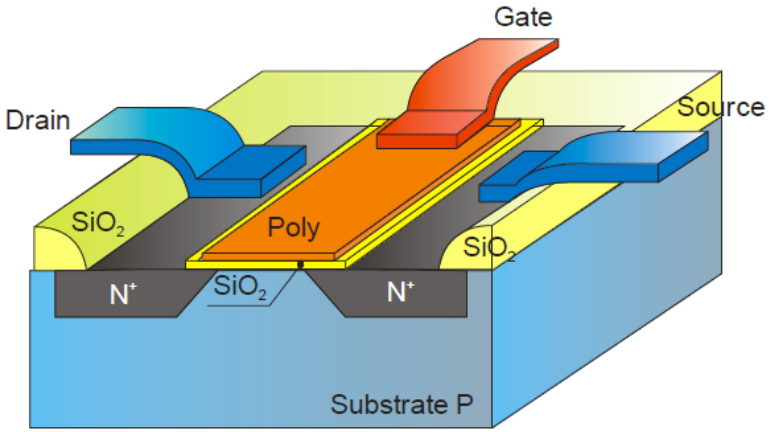
Devices of the basic building blocks

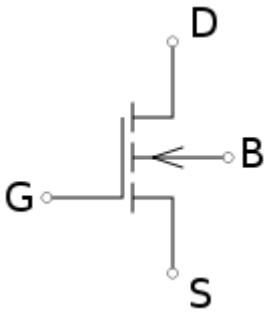
Analog building blocks: MOST

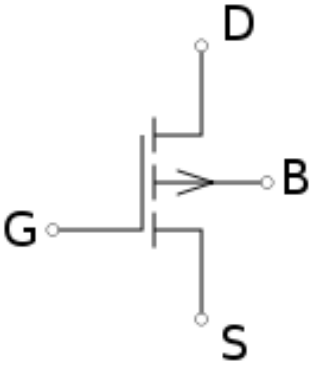
- The most known is the *metal-oxide-semiconductor transistor (MOST)*. The electric field built up between the semiconductor and the metal (called substrate and gate) modulates the conductivity of the space below the gate. That 2D space called channel. The conductivity lets the current flow between the two opposite side of the transistor, called source and drain.

- The basis is the two differently doped semiconductor (more electrons or less appears, the later is called “hole”)
- The typical semiconductor in commerce electronics is silicon.
- The MOST is a four pole (usually three only)
- Source, drain, gate, (substrate)
- The current flow in between source and drain, some leakage current between the channel and the gate, source/drain and the substrate.





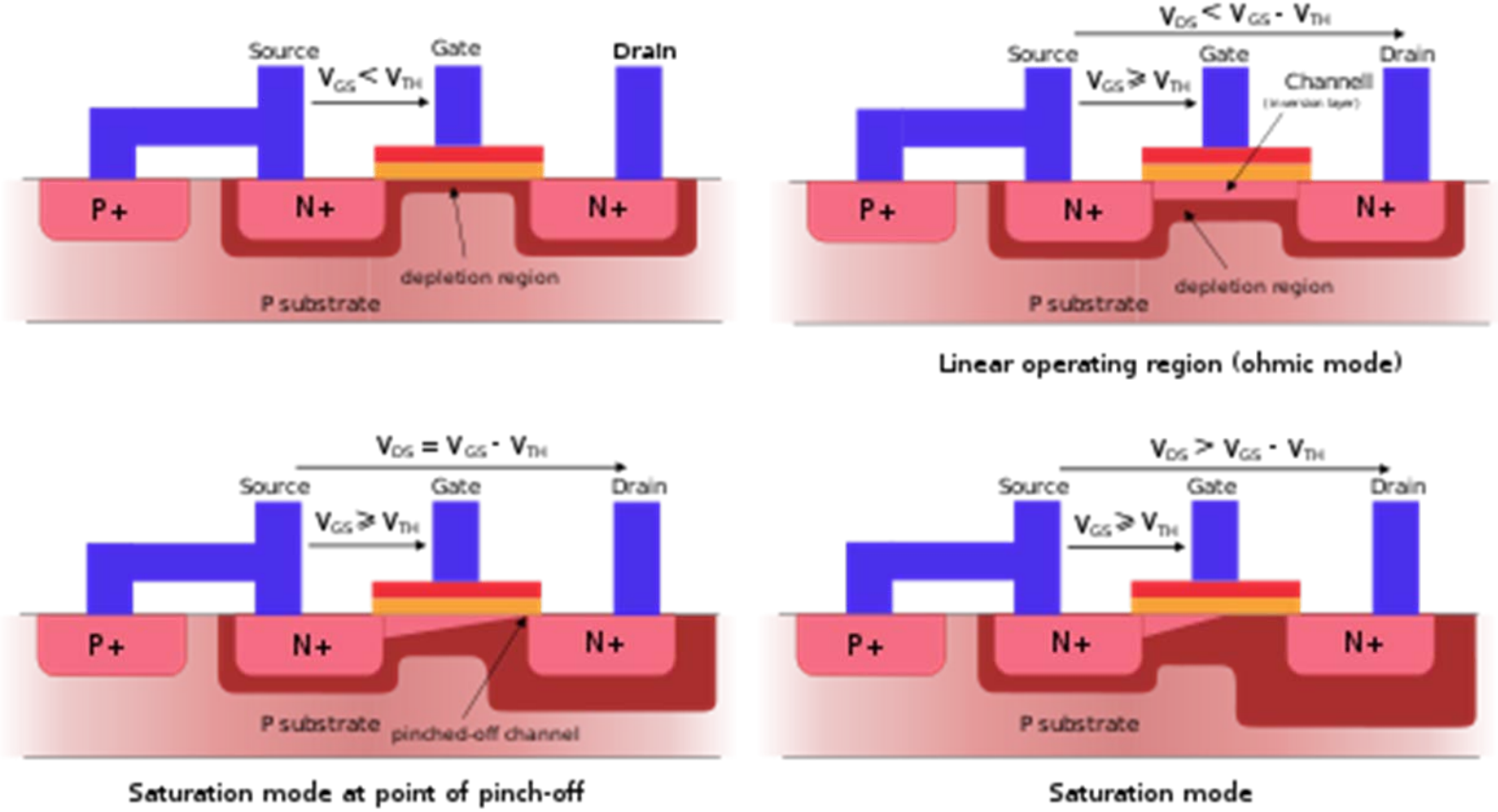




http://commons.wikimedia.org/wiki/File:MOSFET_Manufacture_-_7_-_metalisation.svg

- It a symmetric device, not as the bipolar transistor
- Nonlinear device
- The two different doping called “n” and “p” caused by Boron, P, As ions. In the former, there is electron excess and in the later electron deficit
  - In the P type channels, the hole mobility is 1/3 of the electron mobility
- There are many other semiconductors (Ge, GaAs, GaAlAs, InP, etc.) for faster operation – higher mobility.

Main operating conditions of the MOST transistor: Subthreshold or “off”, linear region, and saturation. Depends on the potential between the terminals.



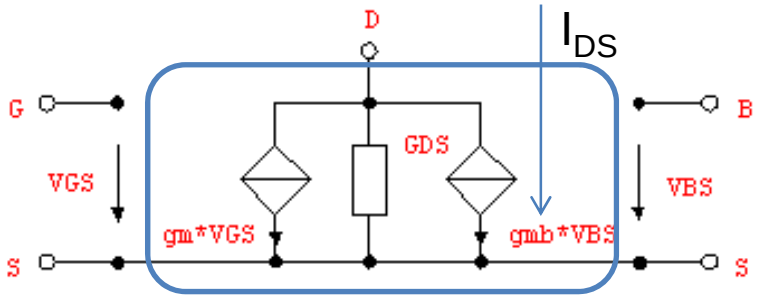
http://commons.wikimedia.org/wiki/File:MOSFET_functioning.svg

- MOST modeling
  - Large-signal nonlinear models
    - Nonlinear, or large signal transistor models fall into three main types
      - Physical models
      - Empirical models
      - Tabular models
  - Small-signal linear models
    - Small-signal or linear models are used to evaluate stability, gain, noise and bandwidth

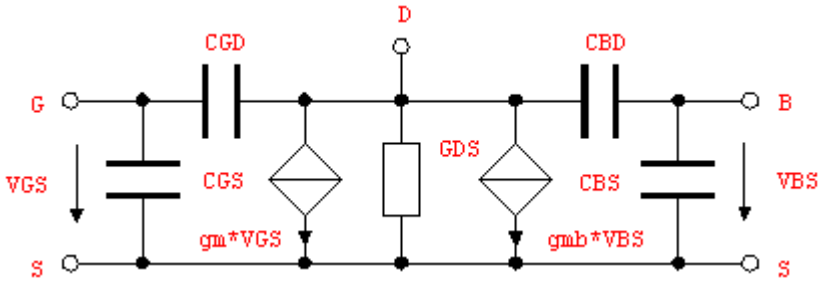
- MOST models, Large-signal nonlinear models
  - Physical models
    - These are models based upon device physics, based upon approximate modeling of physical phenomena within a transistor (oxide thicknesses, substrate doping concentrations, carrier mobility, etc.)
  - Empirical models.
    - This type of model is entirely based upon curve fitting. The parameters in an empirical model need have no fundamental basis.

- MOST models, Large-signal nonlinear models
  - Tabular models.
    - The third type of model is a form of look-up table containing a large number of values for common device parameters such as drain current and device parasitics.
  - Large-signal models for devices continually adjusted to keep up with changes in technology.

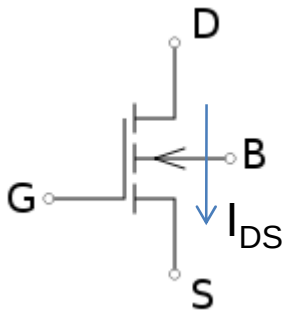
- MOST models, Large-signal nonlinear models
  - Source-drain current is modulated by gate voltage:



DC operation at low frequencies



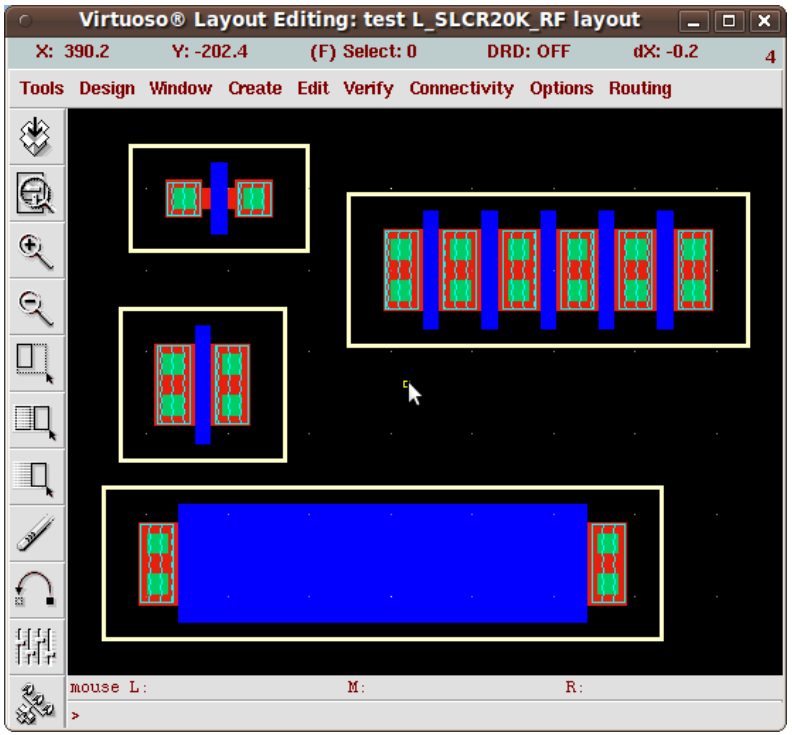
AC operation at higher frequencies



- MOST models, Large-signal nonlinear models
  - The symbol V_{GS} represents the gate-source voltage. V_{GS} is the main controlling factor for the drain current of the MOSFET.
  - V_{BS} denotes the bulk-source voltage.
  - The model parameters of the small-signal equivalent circuits are the transconductance gm
  - The drain-source conductance G_{DS} and the back-gate transconductance gmb, which is considerably smaller than gm.

- Physical dimensions
  - Gate size (width, length: W, L)
  - Source, drain geometry and the contacts
- Technology given parameters
  - Threshold voltage (0-0.7V)
  - Source, drain resistance (<10 ohm)
  - Breakdown voltage (5-20V)
  - Mobility
  - Many second-order effects

- The designed physical properties can be controlled by the CAD tools, usually with parametric templates
  - The size, form (meander, line, fingered), variant (like low power, high speed, high voltage or low voltage).

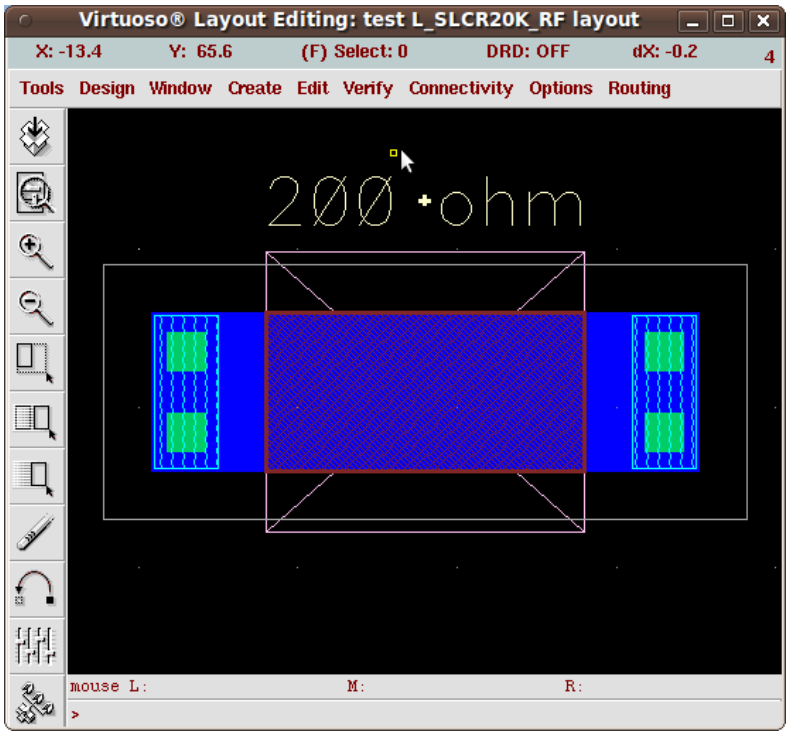


Resistors: Everything has resistivity, so they can be used (the CAD tools can distinguish between wire and metal resistor):

- Metal wires (5-20 mOhm/square)
- Diffusions (100-300 Ohm/square)
- PolySi (100-1K Ohm/square)
- Wells (300 mOhm/square)
- Salicid and no salicid

- Physical properties:
  - Size, similar to MOST, W/L
  - Form (meander, line, fingered)
  - Ending geometry at the contacts (end-effects)
- Technology given:
  - Sheet resistance (Ohm/square)
  - Mismatch parameters
  - Temperature dependency
  - Potential dependency
  - Aging

- The designed physical properties can be controlled by the CAD tools, usually with parametric templates
  - The size, form (meander, line, fingered)
  - Variant (type of resistor like, metal, polySi, well, control of salicid forming to get higher or lower values).

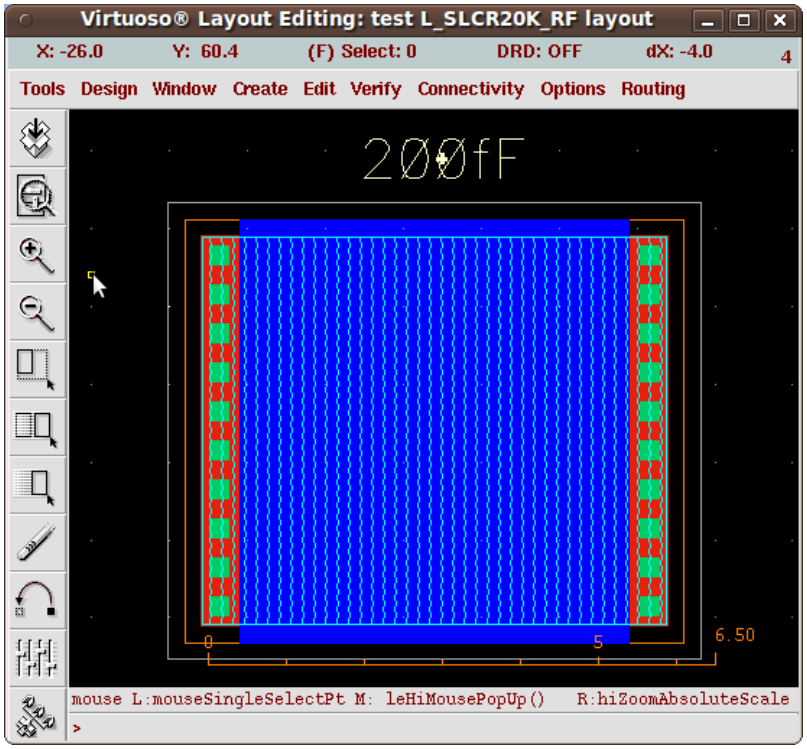


Capacitor: Two conducting layer and an insulator in between is a capacitor.

- MOST, gate and channel, oxide in between
  - Source-drain-substrate shortened, gate the other electrode
  - Large value (~ 1fF/um^2, f means 10^{-15})
  - Nonlinear (V/C, temperature) and slow, but simple
- PolySi to polySi
  - Large value (~ 1fF/um^2)
  - Mostly linear
  - Less common in deep submicron technologies, used frequently in former nodes in analog technologies

- Metal to Metal
  - Large value (~ 1fF/um2)
  - Very linear, fast
  - Very good matching
  - RF and mixed-signal technologies offers it at deep submicron nodes
- Inter digited wire to wire
  - Very difficult to handle in the CAD tools
  - “poor man’s” capacitor
  - Linear, fast, but small value and consume large space

- The designed physical properties can be controlled by the CAD tools, usually with parametric templates
  - The size, form (meander, line, fingered)
  - Variant
  - Value in Farads, and number of repeated blocks, than the tool draw the required size with its connections.

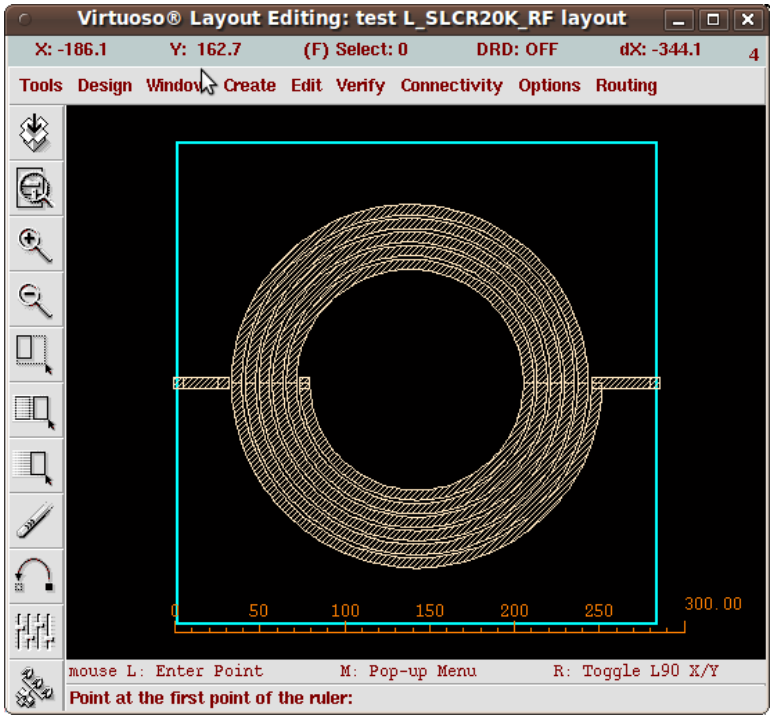


Inductor

The inductor is intended for storing magnetic energy, the inevitable resistance (R) and capacitance (C) in a real inductor are considered parasitics. The parasitic resistances dissipate energy while the parasitic capacitances store unwanted electric energy.

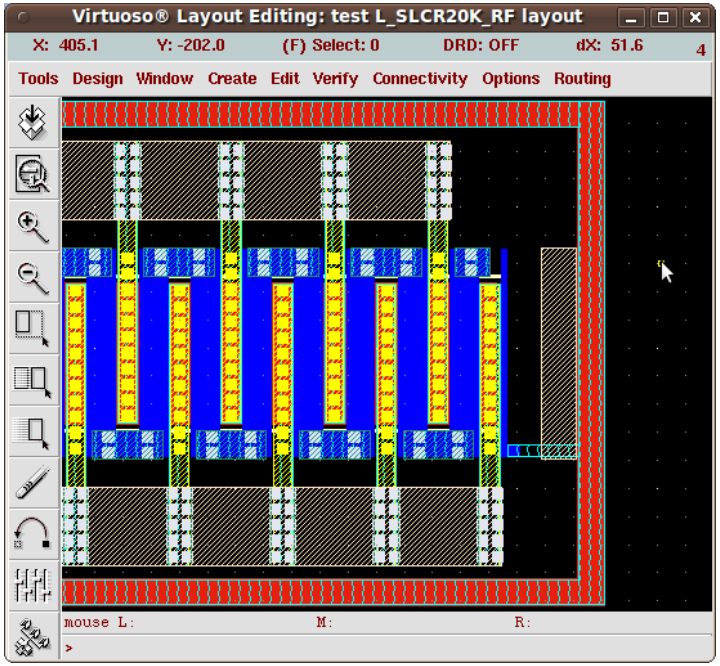
- Used in RF technologies, simply because the available size and value is in the nH range (self resonance ~ GHz).
- Limited inductor quality due to:
  - Limited wire width, interconnect size, and 3D structure
  - Substrate loss (mitigation by patterned ground plane)

- Multi-level spiral structures in the usual wiring
- The designed physical properties can be controlled by the CAD tools, usually with parametric templates
  - These template are barely changeable
  - For given value in Henry, or a to a limited amount, the number of spirals, than the tool draws the required size with its connections.

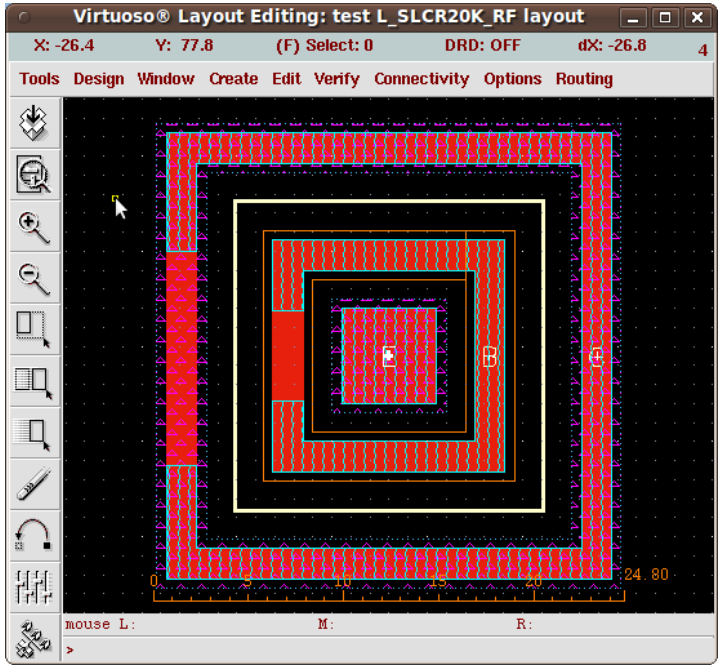


Other exotic devices

- Several other devices can be imagined, that based on any parasitic structure. The changing MOST capacitance is useful for building varactor, the parasitic diodes of differently doped areas gives well controlled P/N junctions, BJT.



Varactor built from MOST



Bipolar transistor from diffusions and wells

Section II

Overview of digital building blocks

Digital design

- What are the design atoms? Gates and connections.
- *HDL* based description (verilog, VHDL, system-verilog, system-C, Handle-C, etc.)
- Random logic, state-machine, register and memory arrays, other complex IP-s
- FPGA or ASIC target. Usually easy to migrate in case of low level description. In complex SoCs it is almost impossible.

IP blocks, anything that has been done by others

- Hardness:
  - Silicon (so called hard)
  - Soft silicon
    - Precompiled for a given technology
  - Soft, just a HDL description
- Buses with blocks of verified protocols
- Periphery controllers (IO, memory, Flash, LCD, …)
- Verification
  - Bus monitor (SoC, PCI, ethernet)
- Software
  - Drivers, communication stacks, OS

Section III

Model and simulation manufacturing imprecision during design

Designed and real precision

- Models
  - MOST models are usually intended to simulate digital (switching and capacitive) transistors only
  - nAmp range operation is not modeled well, paper-pencil
- Operational conditions (temperature) are well handled
- *Manufacturing mismatch* calculation, simulation
  - Called Monte-carlo simulations, barely correct
- Noise models, and simulation
  - Heat, flicker (1/f), shot noise

- Mismatch
  - Given source-drain-gate potential (or resistance, capacitance, etc), the current is different for different transistors, although their design parameters are the same
- Increases with distance of elements (intra-wafer)
- Changes from run to run (extra-wafer)
- Minimal sized elements differ about 10-30%
- Relative precision is much better than absolute!

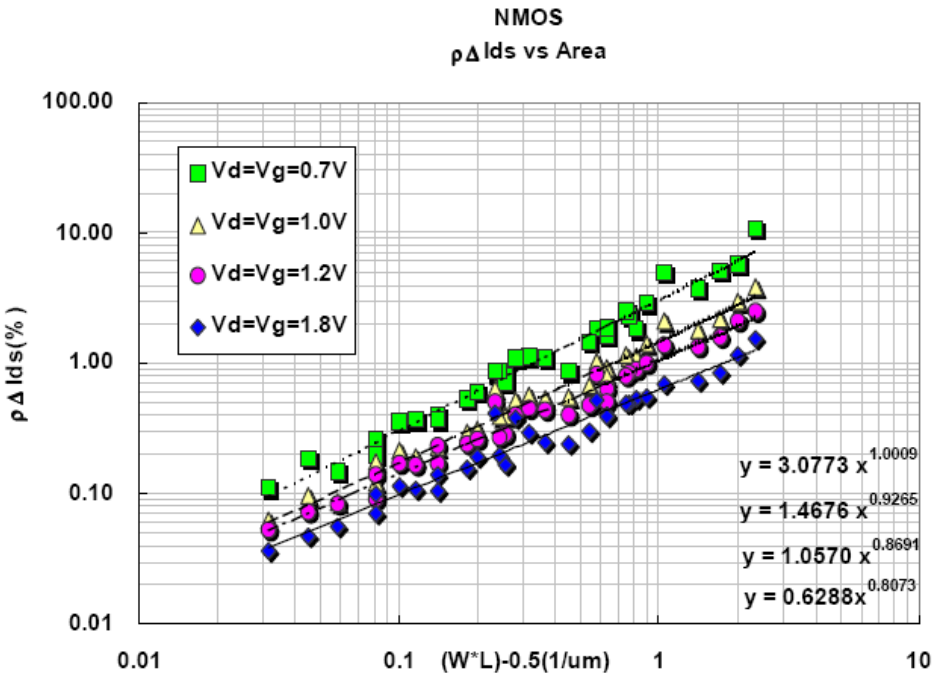
Cross effect suppression is the basis of modular models and design (design reuse):

- In digital systems, the clocking and timing based synchronization hides the glitches and inter period signal propagation, etc.
- In analog systems, cross effects strongly alter expected operation. To mitigate them, one can use special symmetric geometries, increased current, adaptivity, calibration methods, post-manufacturing trimming

Sources of physical processes that impair the performance (referred as to **mismatch**) are highly random effects. The most important are the following:

- Random dopant fluctuation (RDF)
- Line-edge and line-width roughness (LER) and (LWR)
- variations in the gate dielectric
  - oxide thickness variations, fixed charge, and defects and traps
- Patterning proximity effects (classical, and those associated with optical proximity correction
- Variation associated with polish
  - shallow trench isolation, gate, interconnect

- The mismatch has inverse relation with the gate area. The reason for it is that the misaligned edges and limited material volume involved causes the mismatch, as it increases, the average behavior gets „smoother”.



UMC 180 nm technology datasheet.

- CAD tools's simulators in general
  - The simulators can be divided into many categories in general: digital, analog, mixed, small signal, large signal time domain, etc.
  - Their numerical methods, precision can be set – so, there is no optimum for all
  - Numerical nonlinear differential equations solvers can cause convergence and can solve initial condition problems easily
  - There are fast simulators, in which the precision and running time can be balanced

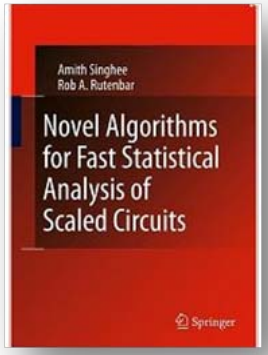
- CAD tools's simulators for mismatch
  - Differences in a local (statistical) and a global (stochastic) component simulation. The former is handled typically.
  - The first studies on MOS technology mismatch were done in the early 80's on capacitors.
  - Next, defined a model that expressed the standard deviation of threshold voltage and current factor with the physical parameter of the MOS transistor.
  - A general parameter mismatch variance model was presented by Pelgrom et al. in 1989 (the mismatch is proportional to the distance of devices and inversely proportional to the area of the device).

- CAD tools's simulators for mismatch
  - Brute force simulation based on Monte-Carlo analysis is simple, precise and widely used.
  - Several dozens to thousand circuits with randomly chosen parameters according to the probability density function of parameters are generated and simulated.
  - The proper correlation and probability density function setting before simulation is difficult and not automated well.
  - Very time consuming.

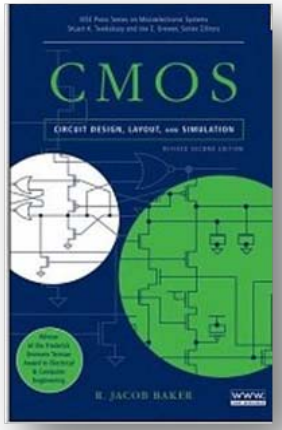
Conclusions

- We went through the most important analog and digital building blocks
- Many different analog devices are usually the same physical entities, operated under different conditions
- The digital design is handled at higher level than analog, but, as a consequence, being restricted at physical level.

Recommended literature



Novel Algorithms for Fast Statistical Analysis of Scaled Circuits
(Lecture Notes in Electrical Engineering)
Amith Singhee, Rob A. Rutenbar
Publisher: Springer; August 7, 2009



CMOS Circuit Design, Layout, and Simulation,
Revised Second Edition [Hardcover]
R. Jacob Baker
Publisher: Wiley-IEEE Press

Comprehension questions:

I. What are the basic building blocks, devices?

II. Draw the cross section of a MOST and describe its parts.

III. What is the difference between designed and manufactured shapes and behavior, what is the source of the difference?