Development of Complex Curricula for Molecular Bionics and Infobionics Programs within a consortial* framework**

Consortium leader

PETER PAZMANY CATHOLIC UNIVERSITY

Consortium members

SEMMELWEIS UNIVERSITY, DIALOG CAMPUS PUBLISHER

The Project has been realised with the support of the European Union and has been co-financed by the European Social Fund ***

**Molekuláris bionika és Infobionika Szakok tananyagának komplex fejlesztése konzorciumi keretben

***A projekt az Európai Unió támogatásával, az Európai Szociális Alap társfinanszírozásával valósul meg.

VLSI Design Methodologies

(VLSI tervezési módszerek)

Connection between designed and manufactured structures

(Kapcsolat a tervezett és a gyártott elemek között)

PÉTER FÖLDESY

The topics covered in this chapter:

- History of CAD tools
- Connection between the designed layout and the manufacturing process
  - Restrictions from manufacturing process yields rules
  - Verification steps of the layout design against the rules
- Constraints coming from the manufacturing imperfections
  - Physical phenomena
  - Manufacturing imprecision

Section I
History of IC CAD tools

History of IC CAD tools:

- 1970, just layout drawing and verification programs. All logic and analog circuits have been hand designed at transistor level.
- Up to Intel 80387 microprocessors have been designed in NMOS technology. These logic circuits based on transistor sizing without clear logic representation.
- At Intel 80286 area, the functional text description (RTL code) appeared. Logic translation to schematic of gates is done by hand!

History of IC CAD tools:

- The clock speed (10-12 MHz) was not fixed, some operations needed more time, resulting in time stretching!
- That was a nightmare for hardware engineers
- 1980, the Intel 80386 appeared using CMOS logic. The timing and functional verification separated. The first automatic multilevel logic synthesis appeared (after the era of PLA gate arrays).

- History of IC CAD tools:
  - First standardized gate libraries are developed with placement and routing tools. Synchronous design with transparent latches (not edge tiggered!).
  - 1986. Intel 80486 was a radical departure. Including cache, floating point ALU, pipelined stages. About 100 people made up the design team. Key was the CMOS and cell libraries, hardware description language, and mapping to gates (at Intel iHDL up to 2005!).

- History of IC CAD tools:
  - Intel Pentium (1993). The bottleneck was the complex control structure and its manual schematic level design and logic translation!
  - Beside the functional checking, the formal verification appeared. Automatic schematic recognition to logic equivalent, and than simulation and verification its functionality (comparison using mathematics!).

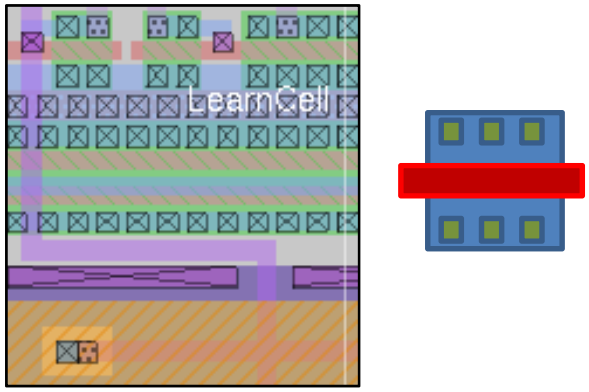
- History of IC CAD tools:
  - Smaller circuits are verified by precise models of extracted parasitics, larger ones using lumped, later distributed, RC extraction and static timing analysis to filter out critical paths. Power grid analysis appeared.
  - Since than the automation increased, higher abstraction, more usage of hierarchy, top-down hierarchical decomposition (divide and conquer), and restrictive methodology.

- History of IC CAD tools:
  - Definitely decomposition of tasks (separation of logic verification from timing verification, separation of logic synthesis from library mapping, and logic designers become programmers).
  - Nowadays the advanced technology nodes generates special constraints, like limited yield, radiation sensitivity, manufacturing imperfection caused statistical mismatch. These issues appears in the tools after strong academy/manufacturer/CAD tool developers.

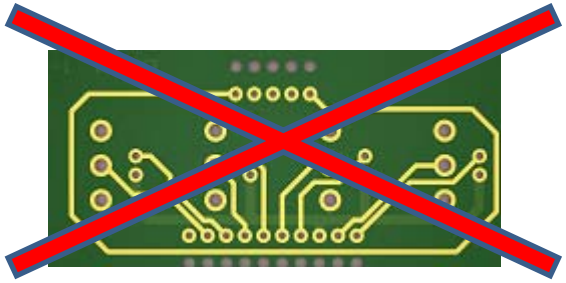
Section II

Relation between the designed and manufactured structures

- Low level design nowadays considers only building from polygons of horizontal, vertical, diagonal (rotation of 45 degree) shapes of given size
  - Mostly rectangle (square) or rarely diagonal shapes
- The reason is the storage requirement of the million shapes, easier automation, easier verification of spacing and size



http://opencircuitdesign.com/magic/



Manufacturing process again:

- Czochralski Process to create single crystal silicon
- Slicing to wafers
- Photolithography methods to create patterns, form on it
  - Including etching of layers to form wires
  - Doping to form ohmic contacts and different active devices
- Finally, slice the wafer to dies and package them into encapsulation

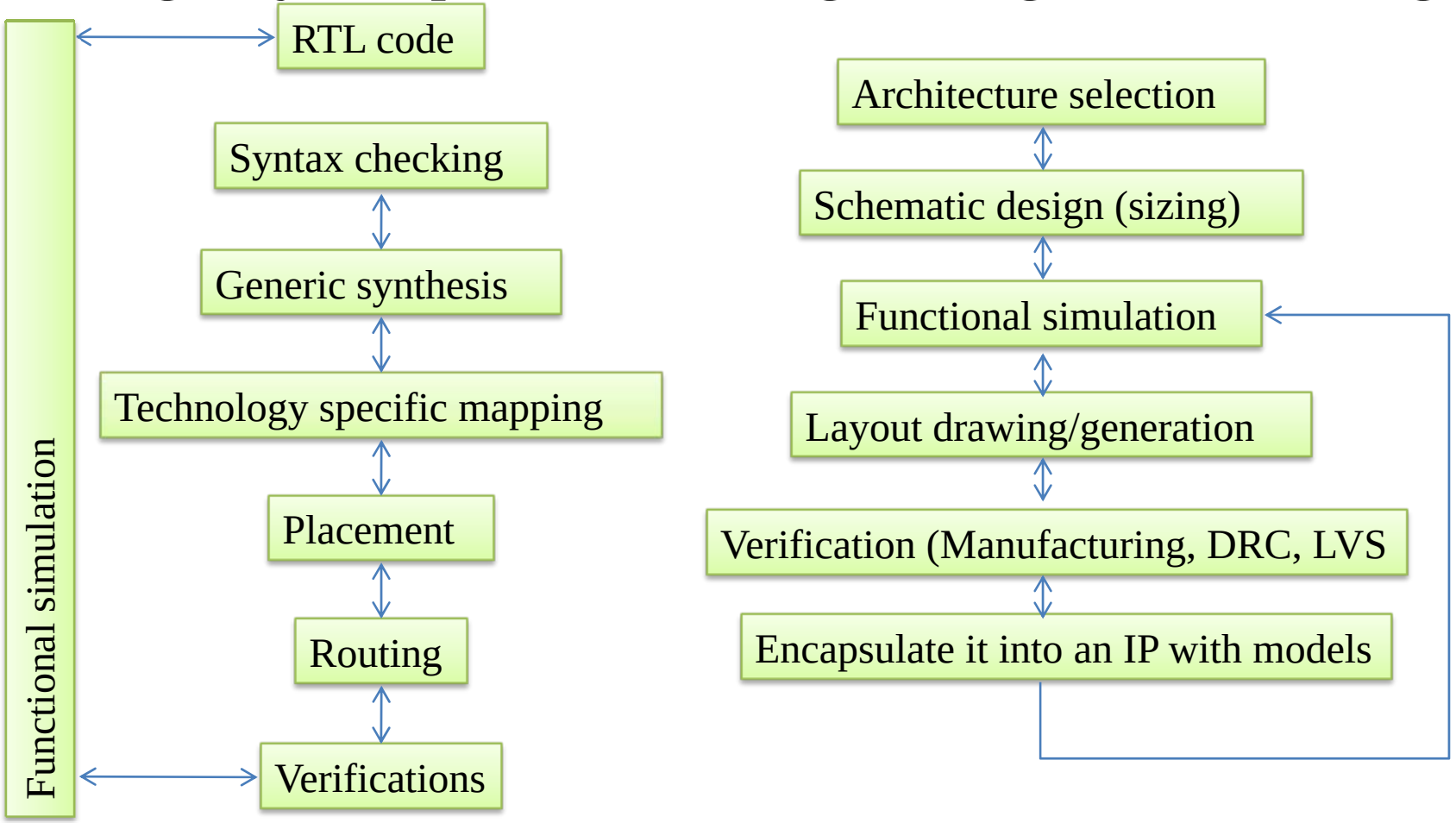
Design style dependents strategies

- Digital design
  - based on verified and characterized layout structures. The goal is to map our design to IP blocks, place them and route their signals. Awareness of timing, power issues.
- Analog design.
  - Usually based on custom designed structures, needs careful design with dozens or hundreds of rules. Building blocks are active devices (like MOST) and wires. Awareness of multi condition operation (temperature, power supply, manufacturing imperfection)

Design style dependents strategies

- *Mixed-signal design.*
  - Combination of digital and analog circuits, including the protection of analog blocks from digital noise. Awareness of multi condition operation (temperature, power supply, manufacturing imperfection) both in analog and digital domain. The more difficult situation due to the mixed simulation and verification tasks.

Design style dependents strategies, Digital and Analog



Digital design's major issues and verification tasks

Topic	Verification task
Functionality	Simulation, Formal checking
Manufacturability	Design rule check DRC
Signal integrity, crosstalk	Electrical rule check ERC Signal integrity check Parasitic extraction
Timing	Static timing analysis STA Statistical STA, SSTA Back annotation, functional simulation
Area	DRC
Routability	Placement and route P&R
Power	Low power design

Analog design's issues and verification tasks

Topic	Verification task
Simulation	Electrical and multimode simulation (spice variants)
Manufacturability	Design rule check DRC Lithography checks Corner analysis
Design integrity	Layout versus schematic LVS
Signal integrity, crosstalk	Electrical rule check ERC Signal integrity check Parasitic extraction
Power	Low power design methods

Classical tasks of the above list is applied sequentially

- Analog design:
  - Plan, draw schematic, draw layout of polygons, check its size, width, spacing, parasitic extraction, simulation
- Digital design
  - Plan, write RTL or higher level description, synthesis to gate level, placement, routing, verification

In deep submicron technologies, these tasks overlap

- RTL based power management
- Routability and placement aware synthesis
- Yield optimization during routing, etc.

Common tasks: Design for manufacturing, including:

- Raw manufacturing constraints
  - Geometrical constraints coming from lithography, doping, etching
- Reliability type rules, in general: Yield
  - Electromigration, hot-electron caused gate distortion
- Operational condition related issues:
  - Electrical current, maximal, peak constraints
  - Self-heating
  - Mechanical stress
  - Aging

Most important geometrical rules:

- Minimum channel width, length of the transistor
- Minimum metal, polysilicon, active, contact, well width
- Metal to metal, polysilicon to polysilicon, active to active, well to well spacing
- Enclosure rules (e.g. metal over contact)

Additional rules:

- Mixed spacing
- Metal fill density (for processes using CMP)
- ESD and I/O rules
- Chip corner rules, etc.

Section III

Source of the constraints is the manufacturing imperfections

Geometrical constraints due to lithography

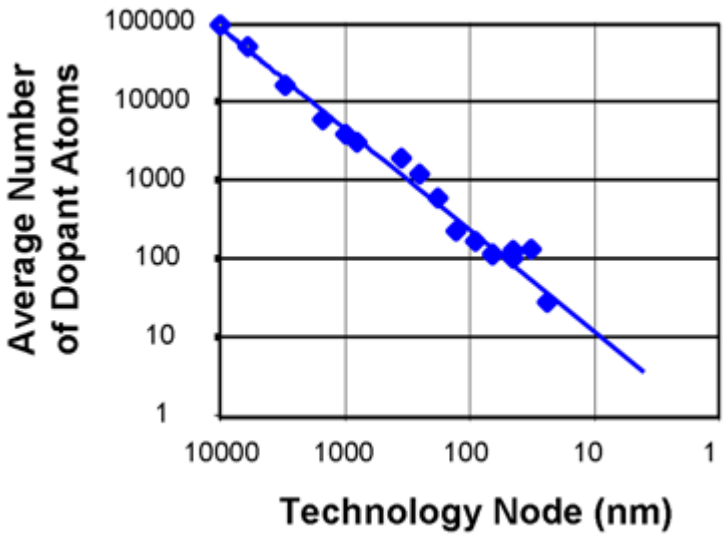
- Size and spacing of objects are restricted by the lithography due to the used wavelength, optics. The safely manufactured minimal polygon size defines the technology.
- A *technology node* is defined by the smallest feature printed in a repetitive array. The half-pitch of first-level interconnect dense lines is the most representative data. The MOST gate width is called *feature size*, and technologies of the same feature size is called *node* (e.g. 1um, 0.25um, 180 nm, 32 nm, 22 nm, etc). Other features are usually larger.
- Between 1 um and 0.25 um, called sub-micron, and below deep-submicron.

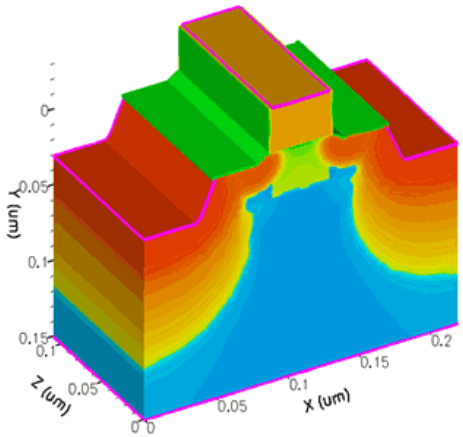
Geometrical constraints due to doping

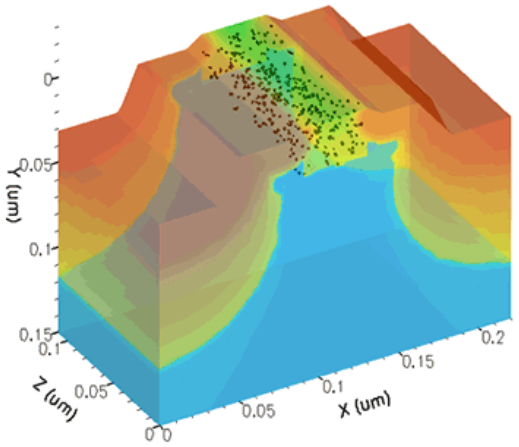
- The doping level is from 1:1e10 to 1:1e4 (the later is the higher).
- The dopants are
  - grown together with the substrate,
  - ion-implanted,
  - diffused.
- The latter two processes are somehow fuzzy, resulting in a not strict borders between the differently doped islands. The result is spacing requirements.
- The higher the doping level, the better the shape (active regions can be placed near the feature size, while wells are spaced in dozens of the minimal feature).

Manufacturing imperfection that spoils precision analog circuits more. The difference between the equivalently drawn devices is called *mismatch*.

- Inversely proportional to size, due to the low number of dopant atoms and the etching process.







http://www.intel.com/technology/itj/2008/v12i2/3-managing/3-sources.htm

Other important reliability (yield) geometrical constraints

- At the edge of the die (chip) there is a need for experimentally verified (and recommended) metal and doping structures to protect the die against sawing, impurity diffusion. This frame is called *scribe line* protection or die sealing rule.
- Due to thermal expansion differences, the wide metals should be slotted not to steer contacts and broke dielectric (called slotting rule).

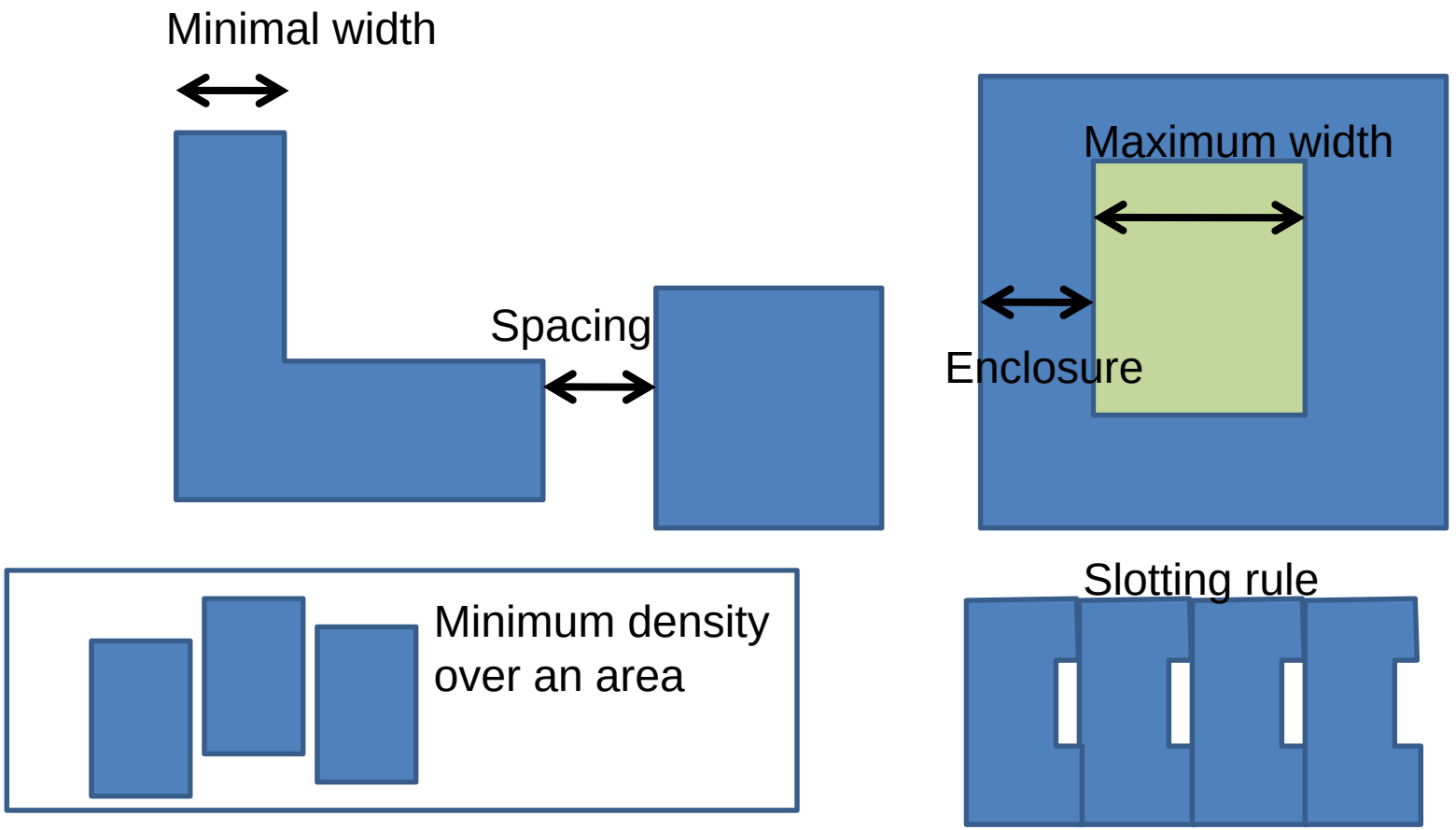
Other important reliability (yield) geometrical constraints

- During plasma etching, electrical charge builds up in the long wires and destroy the connected gate electrodes (like metals in microwave oven). To avoid it, the length and perimeter of connected metals are restricted. It called *antenna rules*.
- In analog design several devices are characterized in given size and arrangement. Hence, they can be drawn in other style, but they will not work as expected. Typical example is the inductor or high precision metal-to-metal capacitor, where other metallization and doping is prohibited in a given environment.

Other important reliability (yield) geometrical constraints

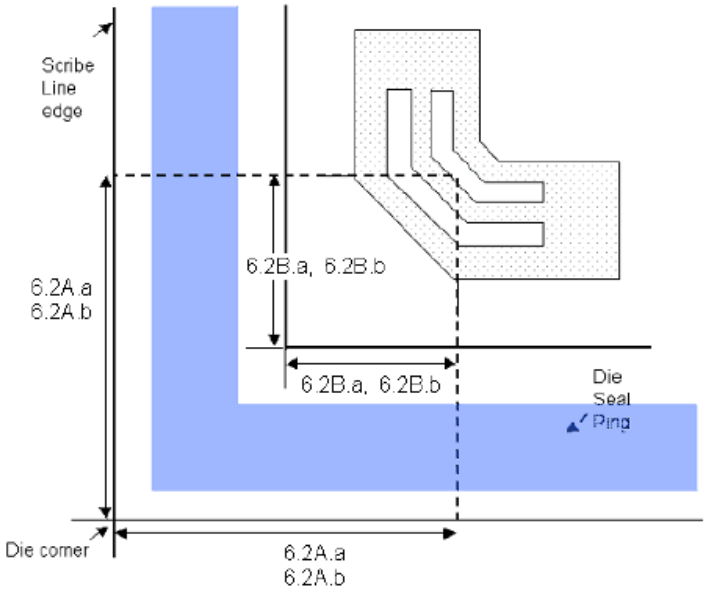
- External requirements can cause rules to be matched. Typically these rules are the wire bonding landing pad size, special sensor devices (no wires above a photosensor).
- For better yield, double contacts are recommended in advanced technologies. Digital synthesis and place and route tools usually support this feature.

Most important geometrical rules



Formalism of the rules

- The rules are well documented and signed with letters and numbers. These codes are consistent from the documentation through the tools' warning and error messages.



E.g. die size and corner rules for UMC 180 nm process:

- Die size < 100 mm2 6.2B.a 125 um
- Die size >= 100 mm2 6.2B.a 340 um

Electrical rules and verification. These rules are not related to manufacturing, but make the circuit operational and safe against the environment.

- Electrical discharge protection (ESD) applied when the internal fine structures are connected to the enviroment.
- Isolation distances, usually depending on the operational potential (e.g. N-Well separation should be larger if they are on different potential, due to parasitic diode and tiristor caused latch up).

Electrical rules and verification.

- *Electromigration* mitigation. Where the current density is high, the metal wire becomes thinner, resulting in even higher density, and finally breaks. The rules set maximal DC, AC current for un unidirectional, Bi-directional, single pulse cases.
- Well connection. The typical connection of n-well to power and p-well to ground checks.
- Check for floating wells, wires, active doping.
- Short or broken signal check.

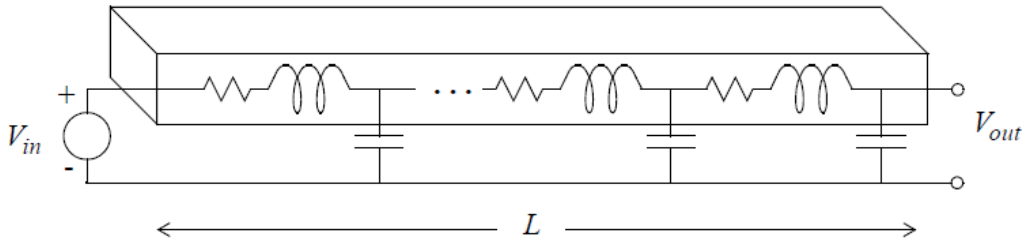
Signal integrity.

- The source of signal integrity problems is cross talk between wires and slow slew signals due to capacitive loads.
- The root of these checks is the parasitic extraction of wire resistances, self and mutual inductivity, capacitance.
- In lower speed circuits or short connections can be avoided, but reaching many 100 MHz operations, becomes critical. If conditions fail, the synchronicity fails or erroneous spikes occur.
- Note that until the time-of-flight is not in the range of rise-fall time, can be handled as discrete model of RC (1 cm – 150 ps).

Signal integrity, voltage slew degrading for a long wire.

Classic wire model

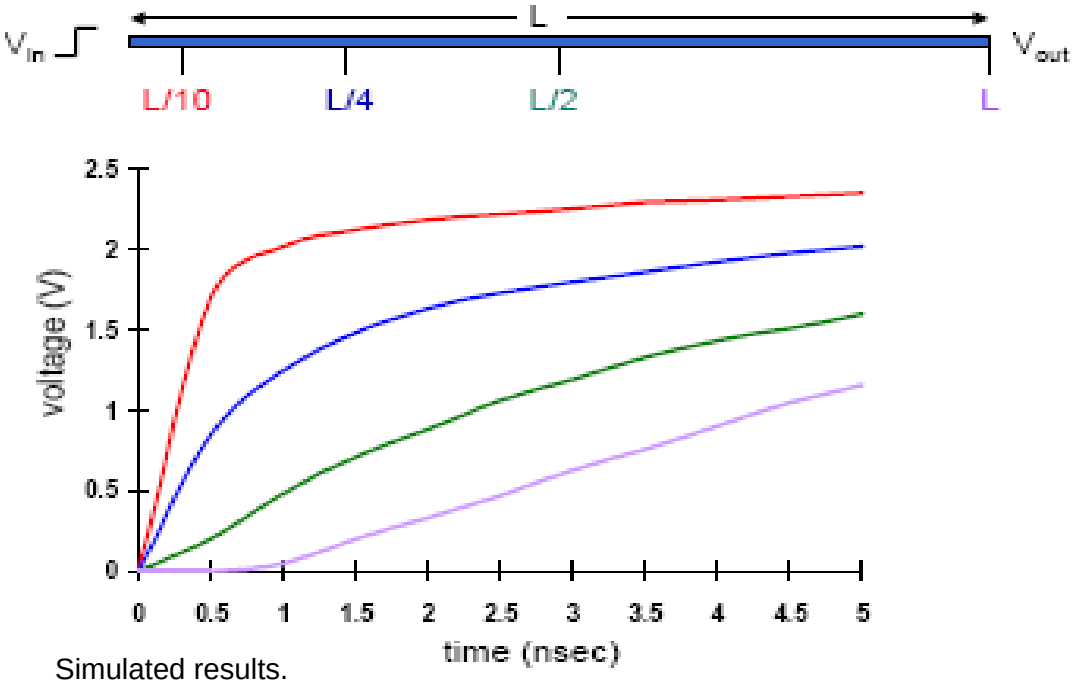
- the conducting wires have parasitic resistance, inductance and capacitance, these parasitic determine how fast signals propagate through the wires. For maximum accuracy RLC transmission line model is used.



Simulated results.

Signal integrity, voltage slew degrading for a long wire.

- What do you think, why this slew rate degradation results in operational failures in “digital” circuits? Hint: think of the thresholding of signals to make binary values of analog.



Simulated results.

A few parasitics that “happen” and a few rule-of-thumbs:

- Typical wire length per random logic IC: 1-2 Km per cm^2
- Typical wire capacitance per cm: 1-10 pF (compared to gate capacitance of a dozen fF).
- Wire delay per mm: ~0.1-5 ns (gate delay ~10-100 ps)
- Maximal wire length if two wires run in parallel with minimal distance: 30-100 um.
- Wire resistance precision: ~30%

Some solution to improve signal integrity and precision:

- Hardware and technology:
  - Better conductors (like Cu)
  - low-k dielectric
  - Wider top metal
- Architecture solutions:
  - Low voltage differential signaling for digital communication (e.g. LVDS)
  - Differential wires in analog design

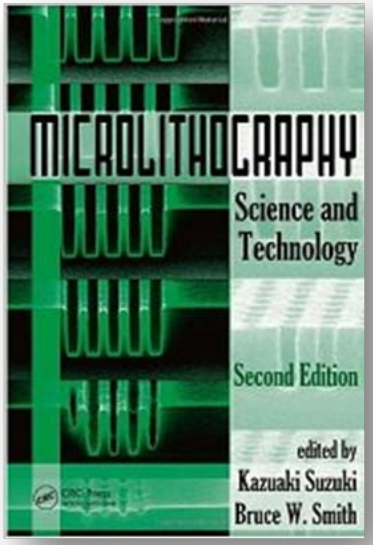
Some solution to improve signal integrity and precision:

- Software and architecture solutions
  - Use of SI aware routing. Use CAD tools to force to avoid situation like long parallel wires.
  - Floorplan. The placement of wide data buses, careful placement of high activity blocks and their shielding.
  - Setting as many constraints for the tools as required. Tools can use these during optimization (like setting false paths to concentrate on the real critical ones).

Conclusions

- We went through the most important design considerations that affects the quality of the produced ICs
- Due to the standardized manufacturing process (that yields the high reliability) the designer hands are tightly bond
- Many physical phenomena affect the performance,
- that are reduced during the manufacturing process by special methods and materials.

Recommended literature



Microlithography: Science and Technology, Second Edition (Opitcal Science and Engineering)
Bruce W. Smith (Editor), Kazuaki Suzuki (Editor)
Publisher: CRC Press; 2 edition (May 11, 2007)

Comprehension questions:

I. Speak about the history of IC CAD tools, what have been the motivating factors?

II. Source of the constraints is the manufacturing imperfections.

III. Analog and digital design tasks.

IV. List the sources and forms of the design constraints.