Development of Complex Curricula for Molecular Bionics and Infobionics Programs within a consortial* framework**

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**Molekuláris bionika és Infobionika Szakok tananyagának komplex fejlesztése konzorciumi keretben

***A projekt az Európai Unió támogatásával, az Európai Szociális Alap társfinanszírozásával valósul meg.

VLSI Design Methodologies

(VLSI tervezési módszerek)

Analog design flow

(Az analóg tervezési folyamat)

PÉTER FÖLDESY

The topics are covered in this chapter:

- Analog/full custom design and automation
- *Schematic circuit* level
- *Layout*
  - Automatic layout generation
  - Mismatch tolerant layout
  - Layout templates
- Effects that make analog design difficult
- Interconnection and constraint driven flow

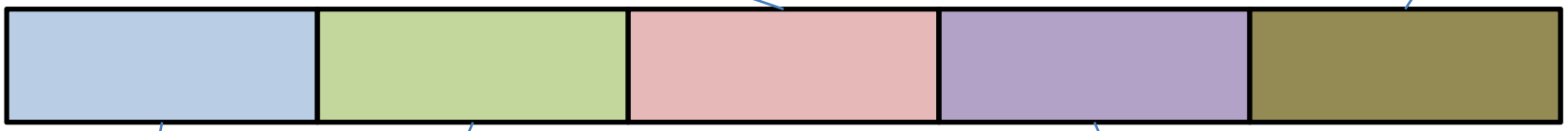
Section I

Analog/full custom design flow and possibilities of automation

Description of mixed-signal systems

Standardized cell and IP level, consists of useful modules, like photosensor layout

HW/SW codesign like converters or processors



System level, expressed in analog or mixed-signal hardware description languages like Verilog-AMS

Circuit level, provides very detailed operation for sensitive modules, like high speed ALUs. Also used for characterizing cells that are used later as black boxes with timing, etc. information.

Physical level, technology and material sciences
Provides physical models for simulation

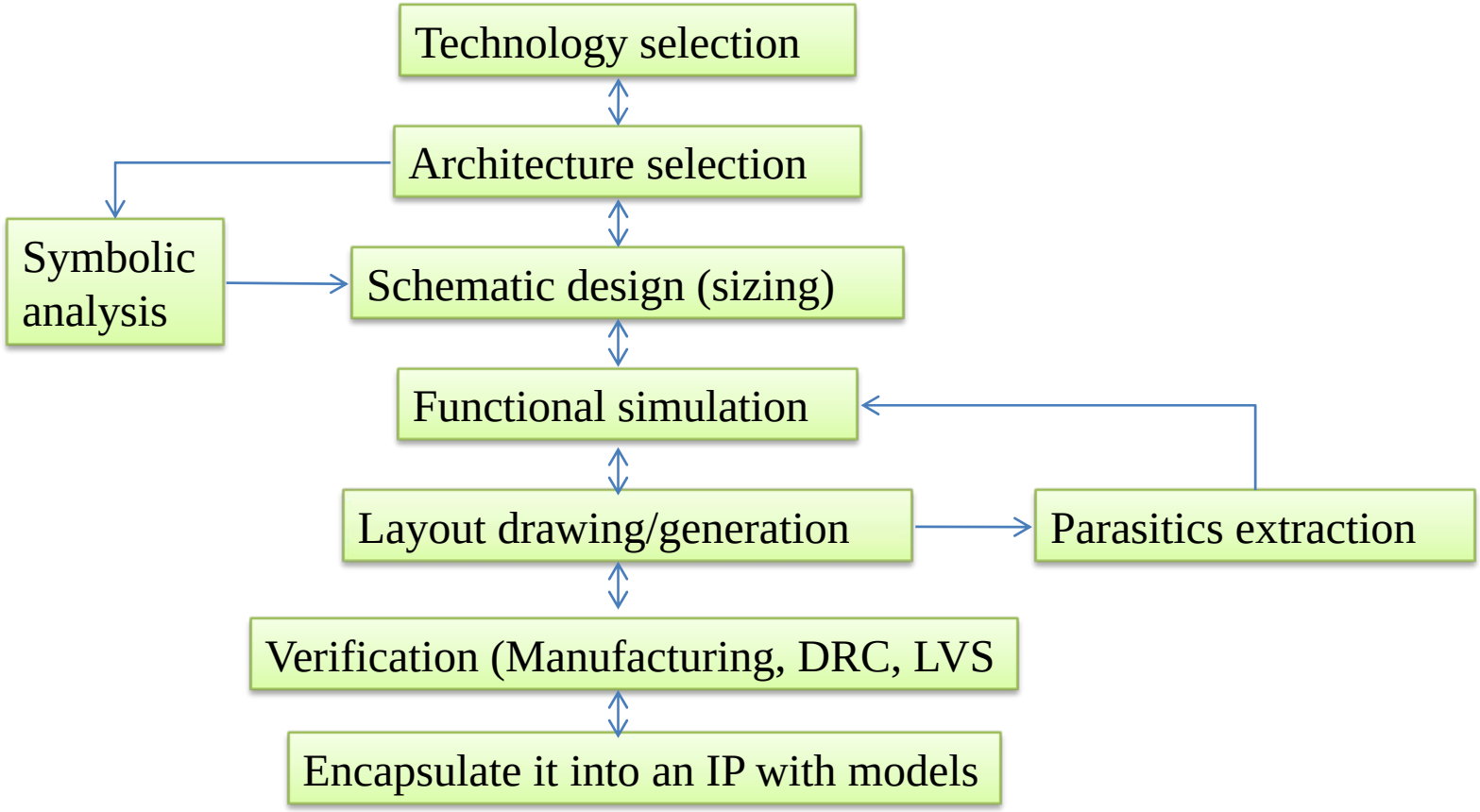
Areas of the full custom design

- System design and verification
  - High level analysis, simulation acceleration,
  - HW/SW codesign,
  - design space exploration,
  - low-power verification (MATLAB)
- Functional verification
  - Simulation with multi-language, mixed-signal codes, parasitic extraction and analyzes,
  - corner and montecarlo analysis,
  - spice and fastspice variants

Areas of the full custom design

- Physical implementation
  - Block implementation,
  - layout acceleration,
  - constraint driven layout
- Manufacturability sign-off analysis
  - Litho-aware, CMP-aware (chemical-mechanical planarization (CMP) can lead to physical or electrical failures),
  - yield analysis

The basic custom design flow:



Question of automation

Digital system synthesis

- Main metrics: propagation time (speed), power, area
- Parasitics: delay, crosstalk
- Analysis corners: a few and more or less well defined
- Linear interconnections
- Building blocks are defined, known, libraries
- Description is standard

Question of automation

Analog system automation

- Main metrics: depends on the circuit (AC, DC, noise, linearity, THM, power)
- Parasitics: …, noise, mismatch
- Nonlinear dependence on parameters, layout, etc.
- Basic devices in theory defined, in practice no, many rule of thumb
- Description is not standard

So, analog circuit automation:

- Generic solution does not exist, only acceleration
- From the variety of systems, the most frequently used are supported by many companies:
  - Operational amplifier
  - SC circuits
  - PLL, VCO, charge-pump, comparator
  - MEMS sensors, actuators
- Design guides
  - There are countless
  - Layout acceleration exists and very helpful
  - Circuit parameter optimization (constraint driven)

Technology selection

- Important, because the generic technologies are usually meant for logic design
  - Imprecise models, no specific high precision cap/resistor
  - Usually the technology pushed to the limit of lithography resulting in very high mismatch
- Options for better analog design:
  - Choice of substrate, that widen or shrink the usable devices
  - Mixed-signal or RF components
  - Special capacitors, resistors
  - Specialties like optical sensor, anti-fuses, flash

Technology selection

- Choice of substrate, that selects the usable devices
  - Silicon or other compound technology (SiGe:C BiCMOS from IHP is used for high frequency design)
- Mixed-signal or RF components
  - Mixed-signal/RF components (e.g. high-Q inductor, thicker top metal layer)
- Special capacitors, resistors
  - Metal-to-metal or polySi-to-polySi capacitor (MIM is usual in advanced nodes, poly capacitor is preferred earlier)
- Specialties like optical sensor, anti-fuses, flash
  - Advanced SOI or BiCMOS process for speed, less noise
  - Optical sensor of good sensitivity needed (most foundry offers)

Architecture selection

- Many rules to follow, but every solution will be different a bit, hard to reuse through technologies
- For an architecture, still many choices (e.g. sigma-delta converter, a vast of options for quantization and feedback method)
  - So, need to go around the design space, exploration
- Specification in tables or in analog HDL

Architecture selection, ways of specification:

- Functionality
  - Conversion bit depth, nonlinearity (INL, DNL, THM)
- Geometry
  - Size, connection points, used metal layers
  - Symmetry, used devices
- Electronic
  - Frequency gain and phase response, DC transfer curve, noise, power, common mode rejection, power rejection

Design, verification automation and helpers

- Parameter tuning for given schematics,
  - usually constraint driven, so metrics should be given (like a programmable calculator), and the parameter refinement tunes the parameters
- Generation of testbench with proper setting, metrics, visualization of results
- Simulation environment generation for
  - Parameter sweeping, corner analysis (temperature, power supply, manufacturing corners), Monte-carlo setup

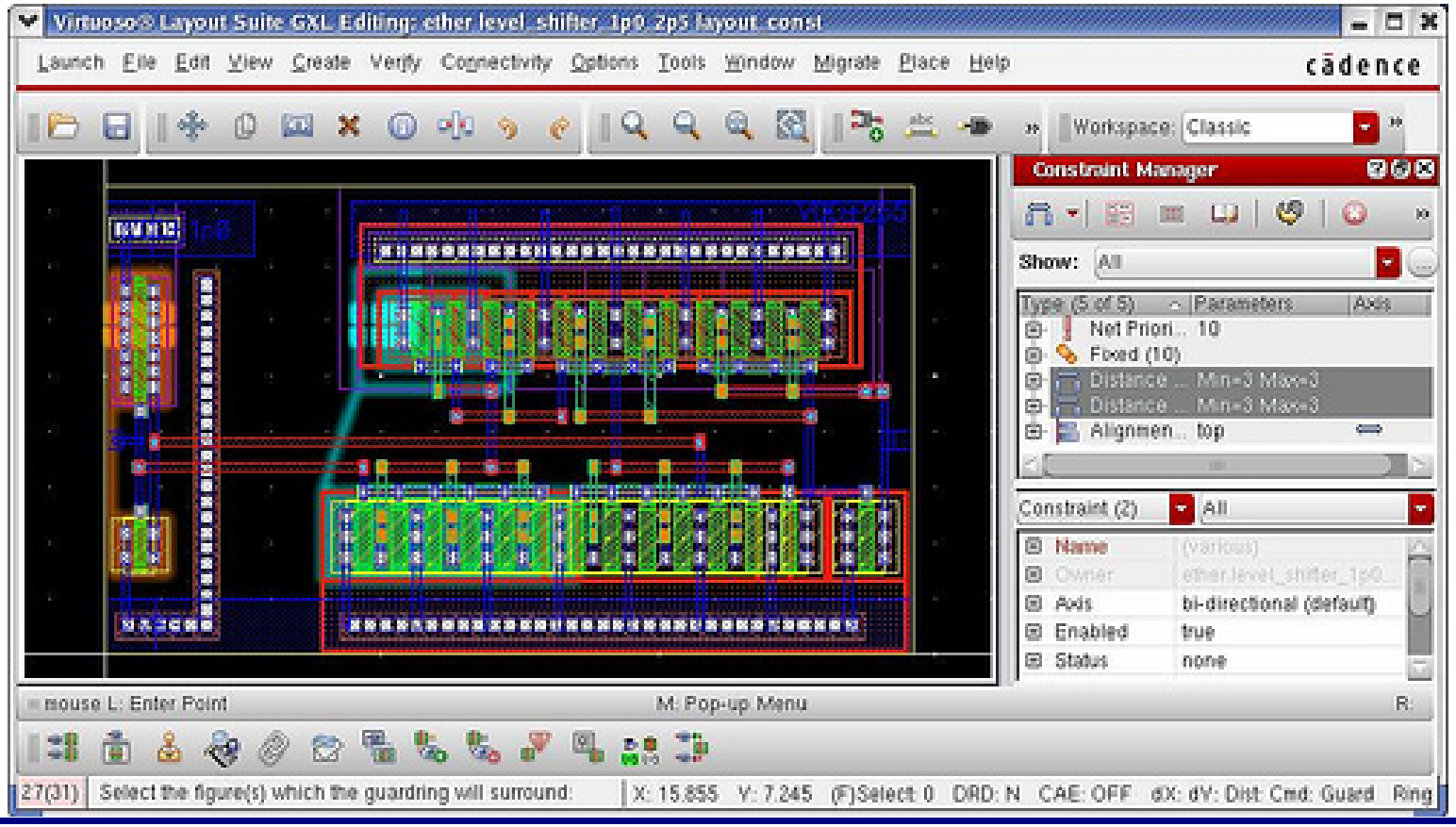
Layout automation, The state of layout helpers is much better

- Full custom polygon drawing utilities
- *P-Cell (parametric cell)*,
  - which are predrawn layout templates that can be resized. They are usually capable of calculations based on the new size (calculating the new capacitor value from size).
  - Exists only for simple structures, like transistors
- IP libraries of simple symmetric structures,
  - like differential device pairs up to complete converters, RF transmitters

Schematic driven layout (e.g. Cadence Layout-XL)

- A method or CAD tool for helping layout drawing
- From the schematic the tool generates the devices and ports, wires in the layout plane (no placement!)
- Handles hierarchical designs
- Can fold and merge transistors
- Real time verification of connectivity, device parameters, etc during drawing

A screenshot of the Cadence virtuoso layout XL editor showing constraints, parameters



Verification of the layout

- The most important verification is manufacturability, and than its functionality
- The important and basic manufacturability check is the design rule check (DRC). Verification of line width, spacing, enclosure, coverage, metal slotting, antenna rules
- The other most frequent check is the layout versus schematic (LVS) comparison. The tools extract the layout and compare its devices, connections and parameters.

Section II

Specialties of the analog design

Specialty of analog circuits

- There are three important issues that destroy ideal operation of our „perfect” circuits:
  - Manufacturing mismatch
  - Noises that are caused by physical phenomena
  - Cross effects between devices through the substrate, come from the digital environment

Mismatch

- The current, capacitance, resistance values are different from device to device, although their design parameters are the same
- Increases with distance of elements (intra-wafer)
- Changes from run to run (extra-wafer)
- Relative precision is much better than absolute
  - The relative precision of several devices placed close to each other is almost perfect
- Symmetric arrangement

Noise sources

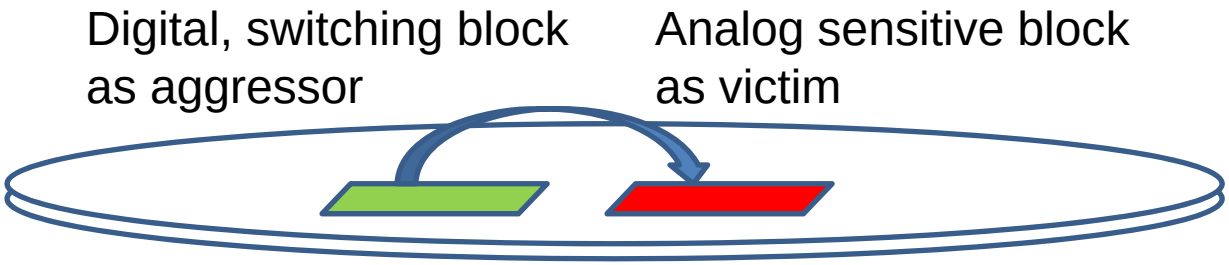
- The noise of bulk CMOS devices is dominated primarily by two noise sources: thermal noise and flicker (1/f) noise.
- Additional sources present are shot noise, generation/recombination noise, and “popcorn" noise.
- Note that the thermal noise ($V^2 = 4kTR$) and shot noise ($V^2 \sim$ current) are physically fundamental of the device and are always present.

Noise sources

- Noise appears in capacitors (e.g. a switch capacitor filter is charged, its potential will be uncertain). This is described by kT/C.
- The kT/C noise really isn't a fundamental noise source, but is actually thermal noise in the presence of a capacitor.
- Image sensors in which, we count electrons instead of volts, the kTC noise is more frequently expressed (Q2 = kTC, usually expressed in units of electrons-squared per Hertz)

Cross effects between devices through the substrate, come from the digital environment

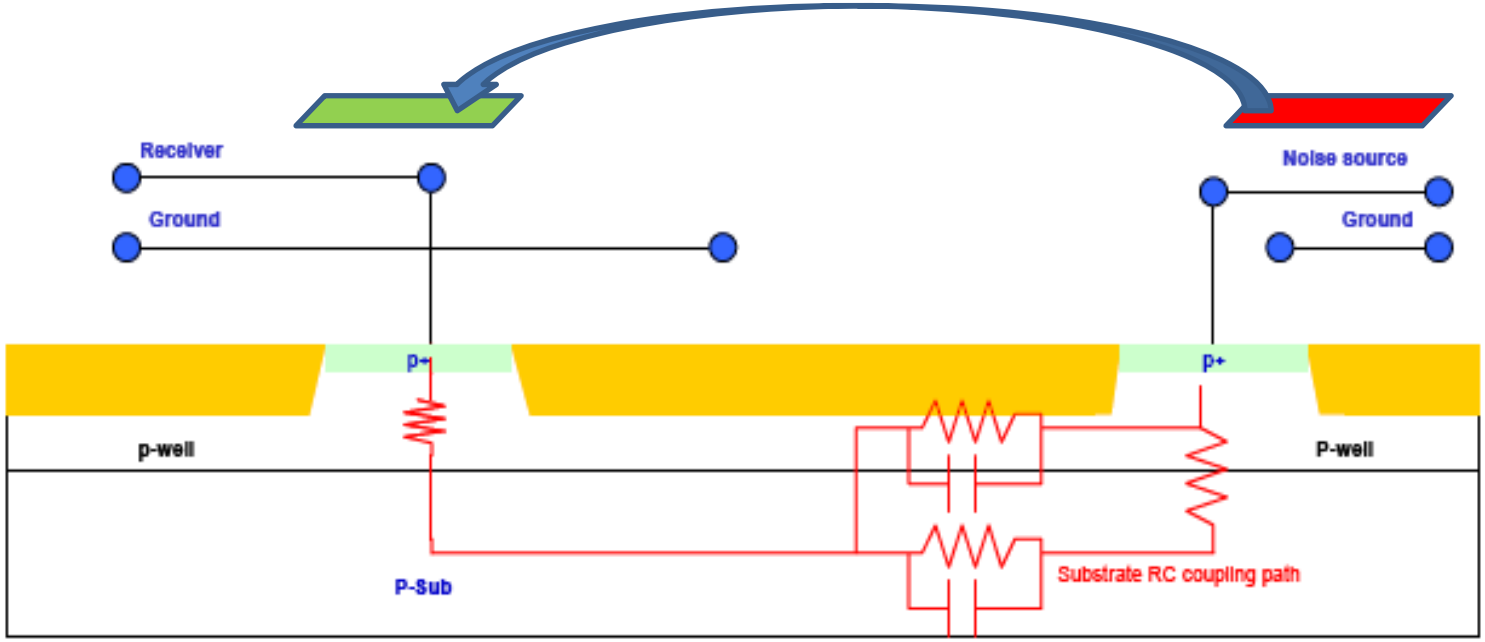
- The substrate on which the devices are placed is conductive (in bulk silicon).
- Digital signal changes send noise to sensitive analog inputs. The most important path for this noise is *substrate coupling* (apart from power lines)



Cross effects between devices

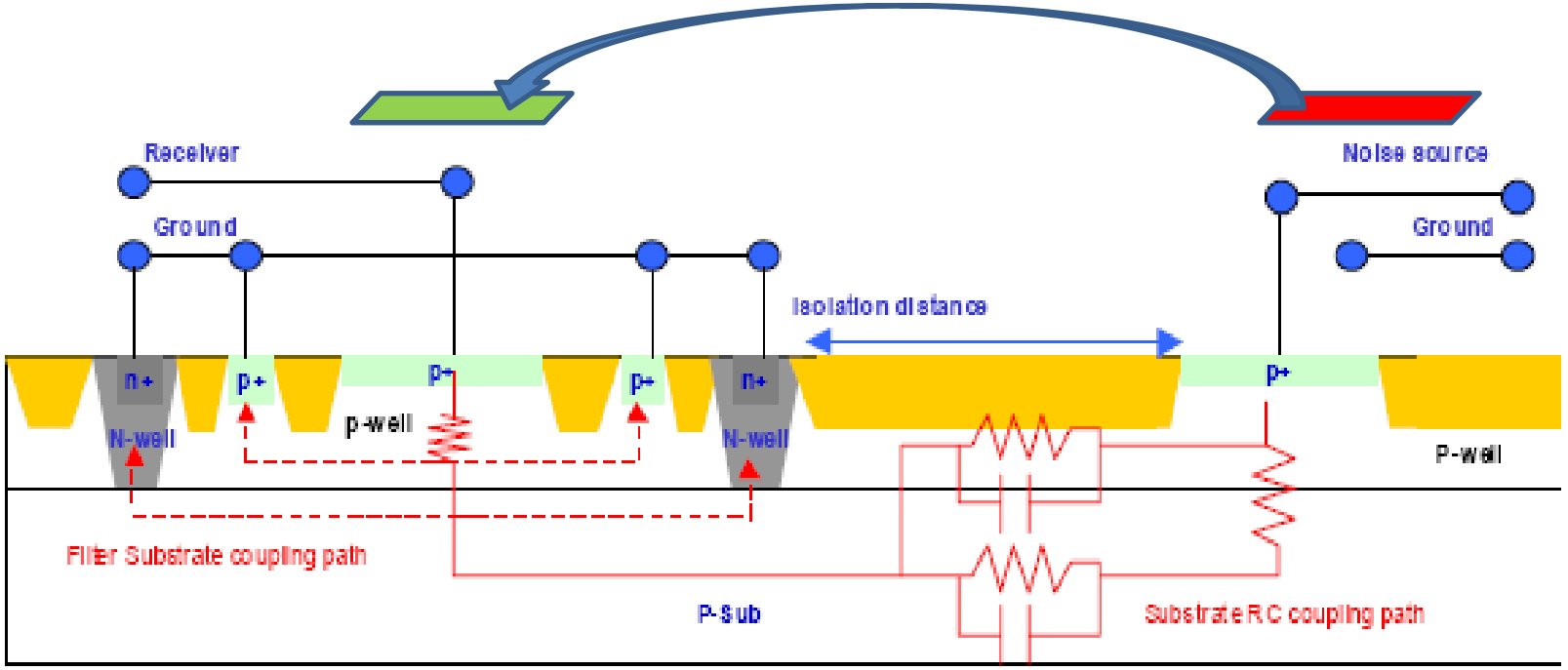
- A techniques are used to attempt to block or cancel this noise coupling:
  - fully differential signaling,
  - guard-rings of wells and doped rings,
  - differential topology of symmetric placement,
  - on-chip decoupling capacitors,
  - triple-well isolation.

Substrate coupling and its mitigation methods by guard-rings



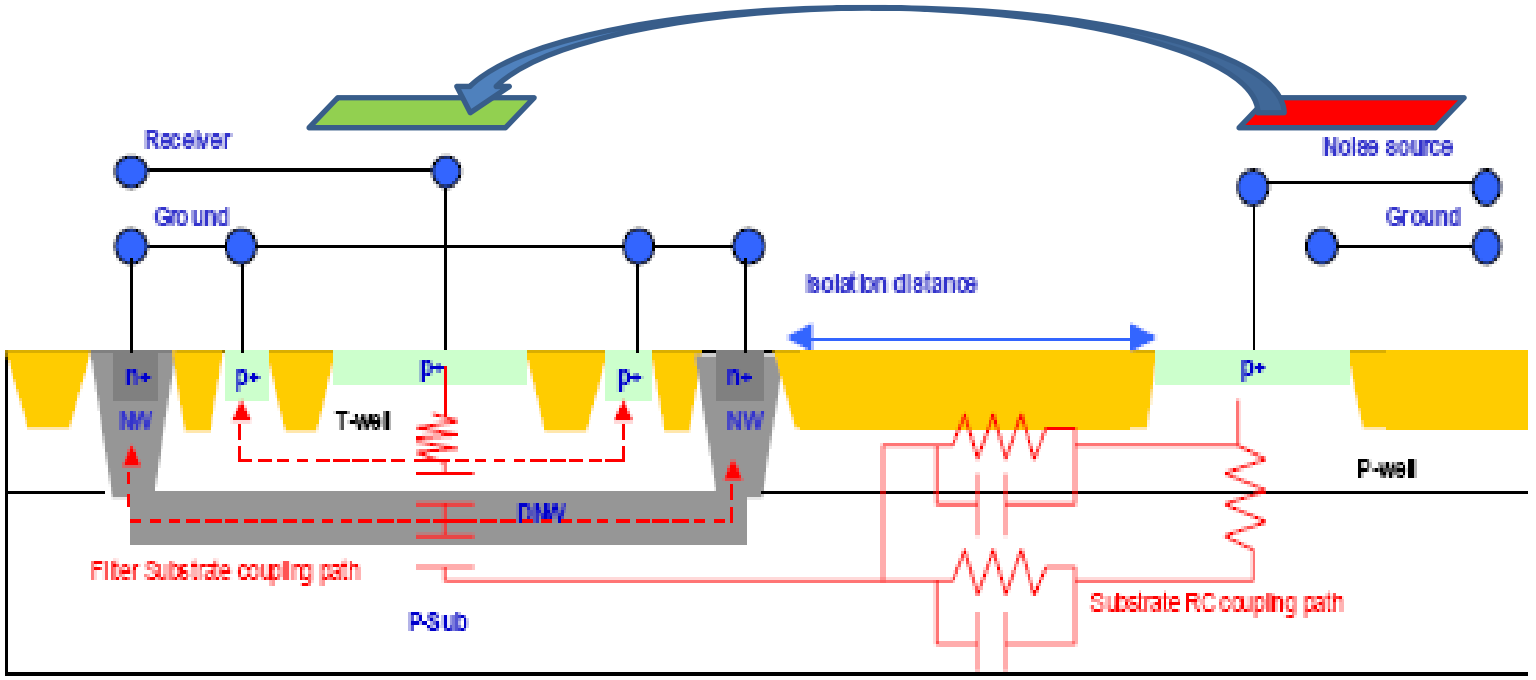
Basic situation of RF noise coupling through the substrate

Substrate coupling and its mitigation methods by guard-rings



Guard ring formed of n-well and p+ substrate connections.

Substrate coupling and its mitigation methods by guard-rings



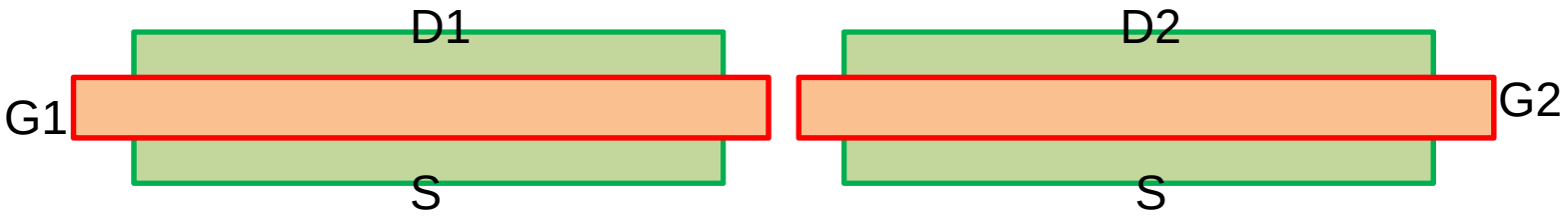
Usage of deep n-well (DNW) to create a guard “plate” under the devices as well. The RC coupling path has several other ways toward the ground level, reducing the victim’s noise significantly.

Techniques of symmetric arrangement

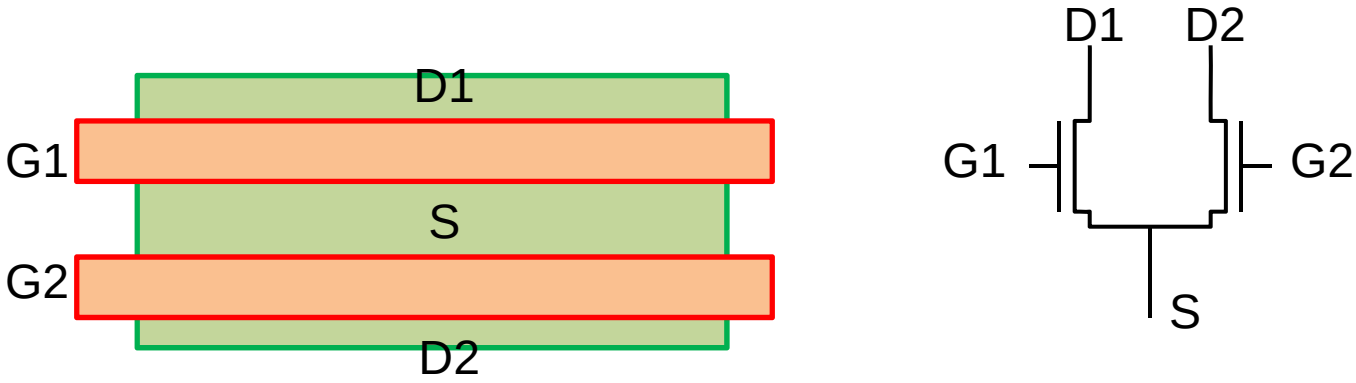
- All of these methods intend to mitigate the gradient like imprecision
- Split devices (transistor, resistor, capacitor) to equal parts and place them symmetrically.
- To make a double element, use two identical
- Every device has the same current direction
- No curves or 45 degree gates or shapes are used
- Dummy transistors or shapes are placed not to make active elements to be on the edge!

Techniques of symmetric arrangement

- Multifinger transistors and the common centroid arrangement



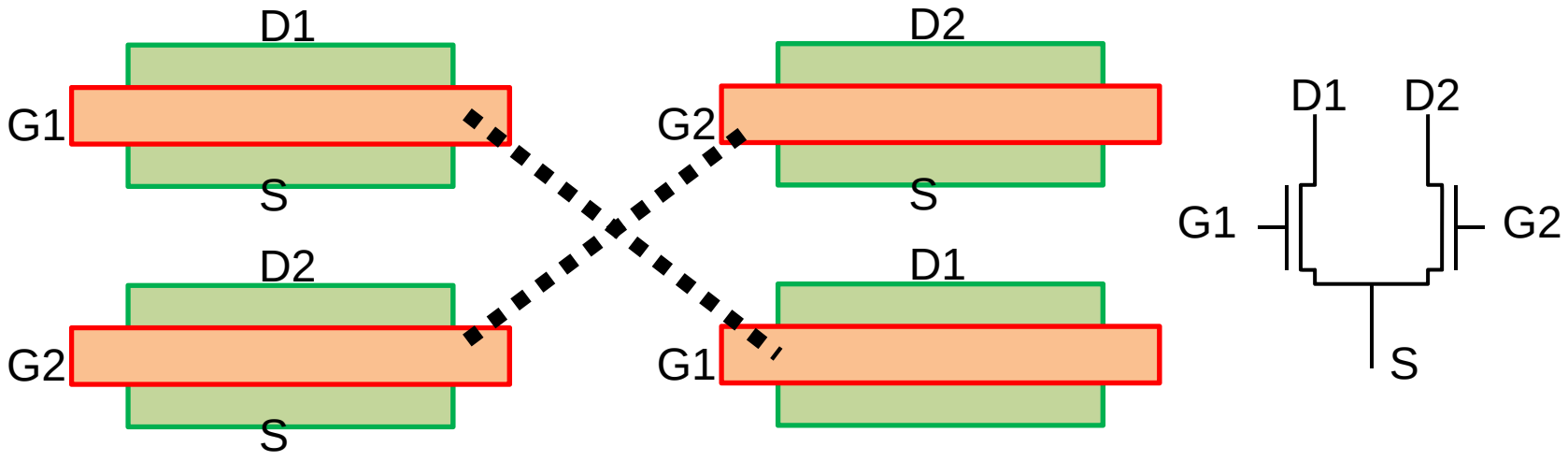
Bad due to cross-chip gradients



Bad due to different current direction

Techniques of symmetric arrangement

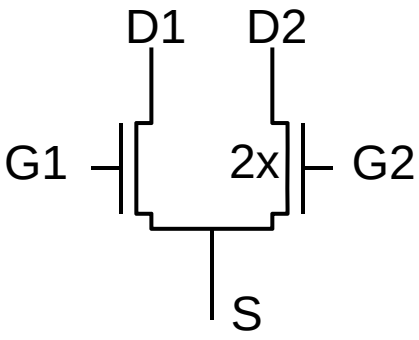
- *Common centroid arrangement*

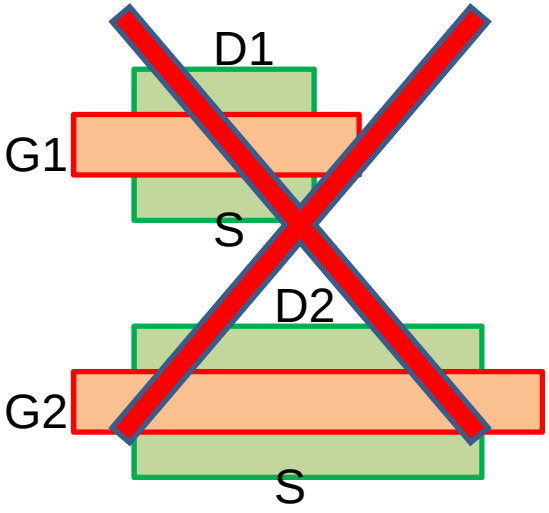


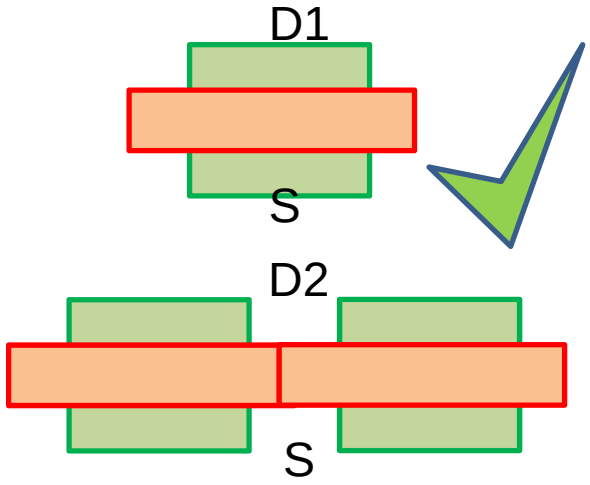
This cross arrangement makes them immune from cross-chip gradients.

Techniques of symmetric arrangement

- Split larger devices to smaller, unite elements!



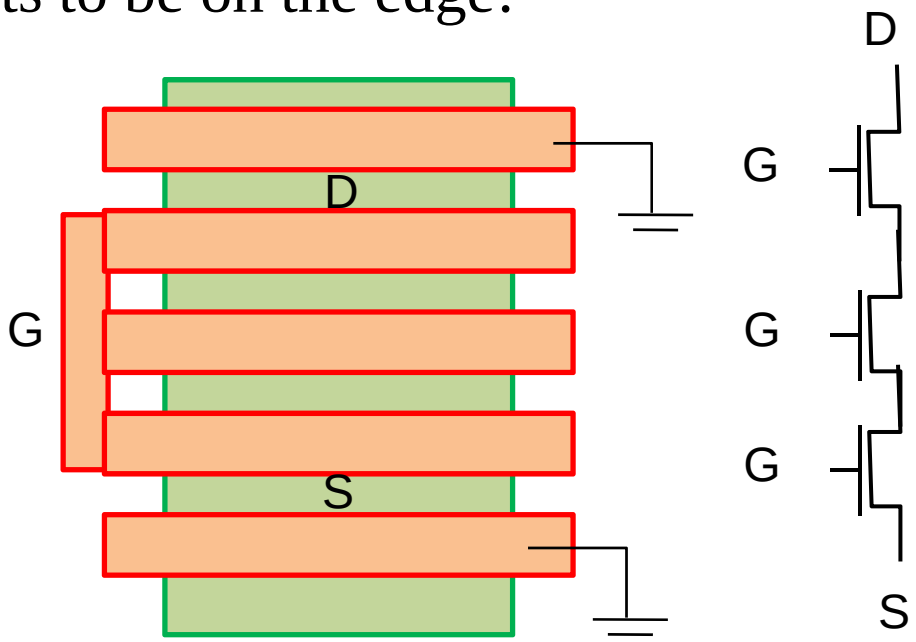




The equal topographic arrangement helps to make them identical.

Techniques of symmetric arrangement

- Dummy transistors or shapes are placed not to make active elements to be on the edge!



This topographic arrangement helps to make them physically uniform.
Remember the limits and mismatch of the photolithography!

Techniques of symmetric arrangement

- *Multifinger transistors*, where large transistors are separated to parallel devices.
- The MOSTs can be connected in this way, but the bipolar ones cannot be. Why?
- Remember the thermal coefficient of the them, in MOST the increasing temperature results in decreasing mobility and decreasing current. In bipolar transistors the effect is in the reverse.

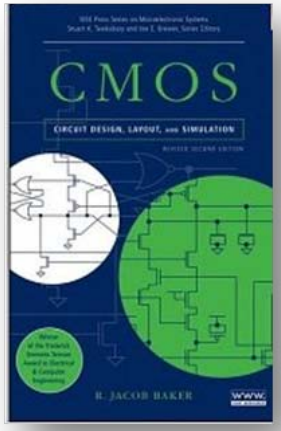
Techniques of symmetric arrangement

- Two MOS transistors can work together as one conducts more current, warms up and the conductivity drops, hence will conduct less current.
- From two parallel BJT the one conducts the higher current become warmer, then conducts even more current, and finally working only suppressing the other one.

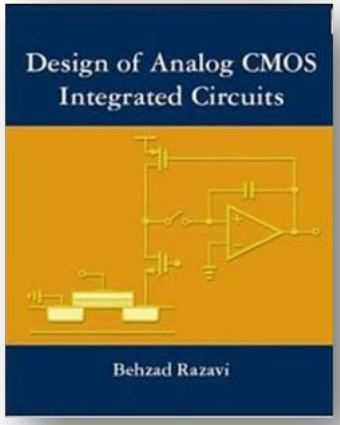
Conclusions

- The analog design is much harder than the digital design
- There are a number of reasons for it
  - Many nonlinear and noise source
  - The devices and interconnections has strong cross-talk
- There is no automatic method for generic analog (full custom) design, but there are several acceleration methods, rule of thumbs

Recommended literature



CMOS Circuit Design, Layout, and Simulation,
Revised Second Edition
R. Jacob Baker
Publisher: Wiley-IEEE Press



Design of Analog CMOS Integrated Circuits
Behzad Razavi
Publisher **:** McGraw Hill Higher Education; First Edition (October 1, 2003)

Comprehension questions:

I. Describe the analog design flow.

II. What is the difference between analog and digital flows?

III. What is the mismatch and how to mitigate its effects?