Development of Complex Curricula for Molecular Bionics and Infobionics Programs within a consortial* framework**

Consortium leader

PETER PAZMANY CATHOLIC UNIVERSITY

Consortium members

SEMMELWEIS UNIVERSITY, DIALOG CAMPUS PUBLISHER

The Project has been realised with the support of the European Union and has been co-financed by the European Social Fund ***

**Molekuláris bionika és Infobionika Szakok tananyagának komplex fejlesztése konzorciumi keretben

***A projekt az Európai Unió támogatásával, az Európai Szociális Alap társfinanszírozásával valósul meg.

VLSI Design Methodologies

(VLSI tervezési módszerek)

Power consumption and low power design

(Kis fogyasztású rendszerek tervezése)

PÉTER FÖLDESY

The topics are covered in this chapter:

- Source of power consumption in digital circuits
- Technological ways to decrease consumption
- System level concerns
- Advanced softmethods and architectures
- CAD tool support

Power has always been an integral part of consumer electronics. Due to green efforts and battery powered electronics, the power consumption is a critical part of the architecture of the SoCs.

At 90nm and beyond the need to save power is no longer optional. It is a requirement by consumers.

For chip architects and engineers at all levels of the design flow, the tradeoffs between area, power and performance are now unevenly weighted toward power.

Section I

Source of power consumption in digital circuits

The power consumed by the CMOS circuits can be divided into three main, different components and further sub-classes:

- Dynamic (switching) power consumption
- Short circuit power consumption
- Static (Leakage) power consumption
- Signal distribution also dissipates.

- *Dynamic (switching) power consumption*
  - Occurs when circuits change their logic state charging and discharging of output capacitor.
- Short circuit power consumption
  - During switching of both NMOS and PMOS transistors in the circuit and they conduct simultaneously.
- *Static (Leakage) power consumption*
  - Off state subthreshold current
  - Diode reverse bias current, drain- and source-substrate junction band-to-band-tunneling (BTBT)
  - Gate tunneling leakage current

- Signal distribution dissipation
  - Every conducting material (except for special cases) consumes energy, heats up and changes when conducting current. This results in two things:
    - Heat conduction shall be solved and the heat and power distribution became the part of the CAD tools
    - The phenomena of electromigration (when metal atoms dislocate due to current) is a serious issue and cause failure.

- Dynamic consumption
  - The dynamic consumption is caused by the switching activity of circuits. It can be estimated by the charged capacitance (remember for low-K dielectrics), the potential change, and the activity rate of switching activity.

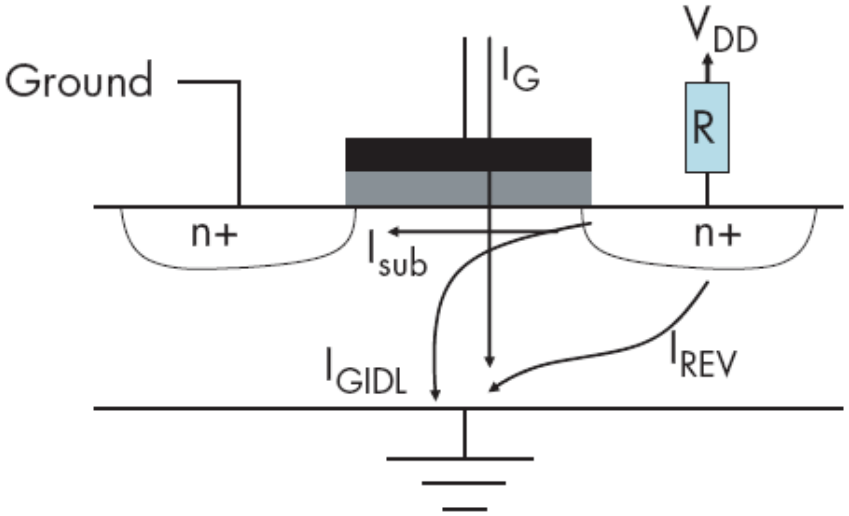
$$P_{dynamic} = \left[\frac{1}{2}CV^2 + Q_{ShortCircuit}V\right] f \cdot activity$$

Capacitance charging

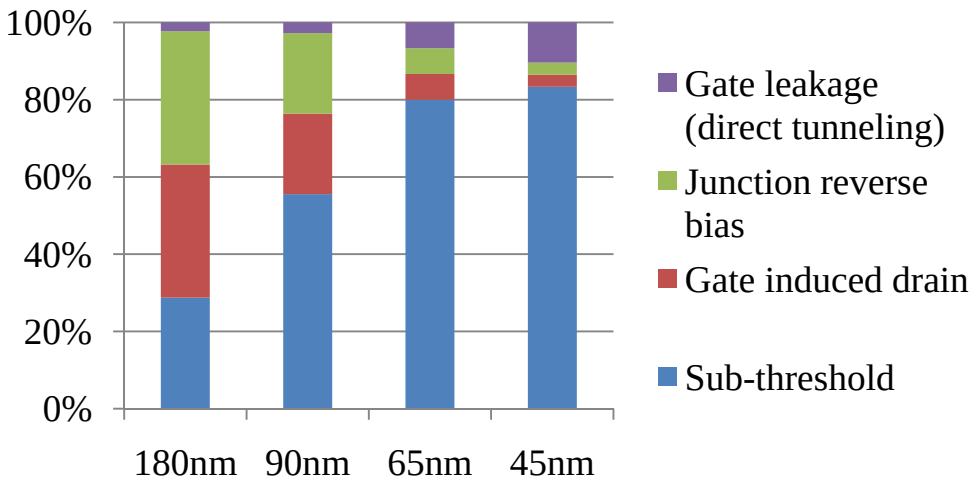
Short circuit charge during switching

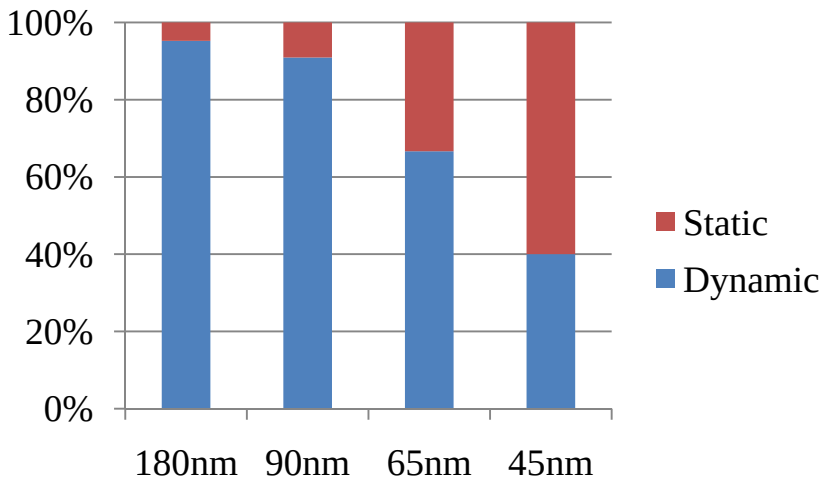
Percentage of circuits That switches each cycle

- Static (Leakage) power consumption
  - Important to see that the components of the static consumption does not depend on the operation speed, but on mostly technological choices:
    - threshold voltage – controlled by technology
    - electric field – dominated by the oxide thickness and signal level



- As technology node shrinks 65 nm and below the leakage (i.e. leakage current and gate tunneling) increases and become dominant owing to lower threshold voltage and the increased electric field, respectively.





Task: estimate the dynamic power consumption of a hypothetical CPU described the following data:

- Transistor count: 1e9
- Switching activity: 1%
- Clock speed: 2 GHz
- Core power supply: 1.2 V
- Average gate load: 50 fF

After calculating the result, the followings will show how to reduce this value.

Section II

Technological solutions to reduce power consumption

Technological modifications to the classical CMOS technologies to reduce consumption

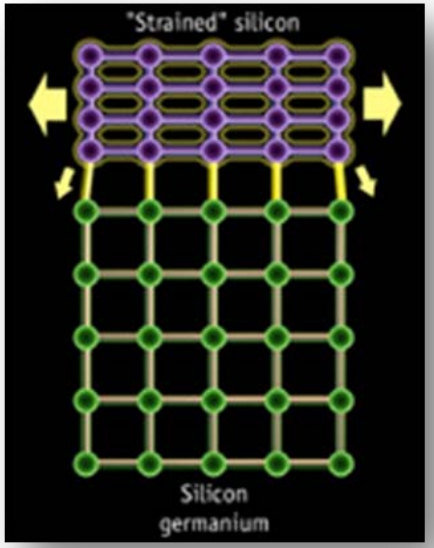
- Gate oxide
  - Leakage could be minimized by having a higher capacitance between the gate and the channel. This is achieved by
    - Increasing the dielectric constant (K) of the gate dielectric
    - Making gate oxide thinner
  - The later method worked so far, but thinning the gate dielectric increases gate tunneling current exponentially (at 65 nm gate oxide 2 nm!)

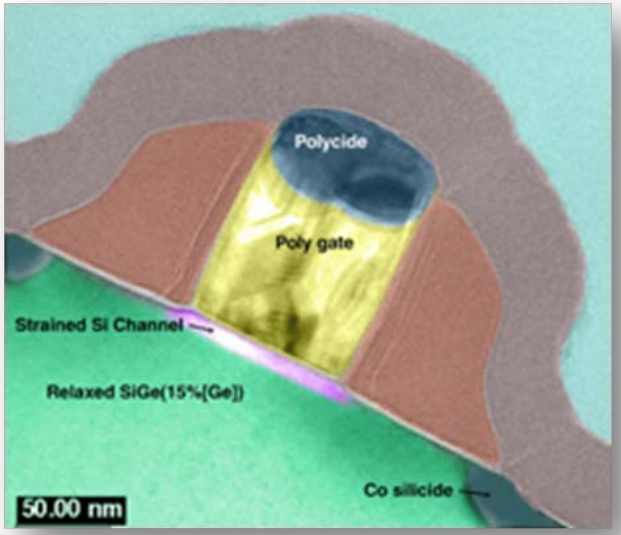
- The high-K dielectrics, such as SiN_x, hafnium dioxide (HfO_2), zirconium dioxide (ZrO_2) and titanium dioxide (TiO_2), RuZrHfO, are introduced below the 65 nm node.
- The drawback and challenge with new high-K thin dielectrics is that it is not compatible with poly-Si gates and its Boron dopant atoms diffuse through the thin oxide.
- As a solution, new, metal gate material appeared made of "magic" composition containing mostly hafnium, rubidium, tantal.
- Dual metal gates are developed for n and p MOST.
- The consumption decreased significantly (100x compared to SiO_2 dielectrics)

- Copper Routing
  - Copper replaced aluminum, providing reduced electrical and power (heat) resistance, and thereby increasing performance.
  - All-copper metallization for on-chip routing appeared with the 150-nm process node, and used below.
- *Low-k Dielectric*
  - A dielectric provides isolation between metal layers, enabling multiple routing layers. This dielectric and the metal layers form capacitors that decrease signal propagation, increase dynamic power consumption.
  - Moving to a low-k dielectric from SiO_2 reduces this inter-routing layer capacitance.

- Triple Gate Oxide
  - The thickness of the gate oxide affects the performance and leakage current of a transistor. It is common to use three (or more) separate oxides (triple gate oxide) across the I/O circuitry and core logic. Two of these are used to enable low-performance transistors with minimum leakage, and high-performance transistors for maximum performance.

- *Strained Silicon*
  - Strained silicon technology, increases the transconductance of the transistor channel, thereby increasing the performance of the transistor. The silicon crystal is strained by SiGe to increase electron mobility.



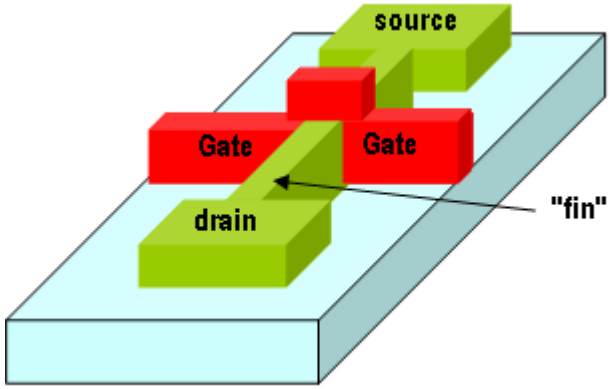


Novel technologies for low power

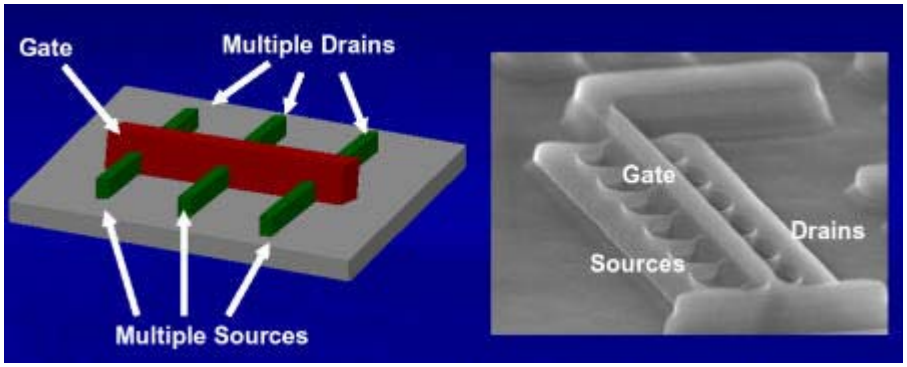
- Dual gate MOSFET
- FinFET
- Radiation hardend transistors (the total dosage increase the subthreshold current)
- Carbon nanotube transistors - they could 20-30x larger on state current.
- Other system components

Double gate FET or FinFET

- The distinguishing characteristic of the FinFET is that the conducting channel is wrapped around a thin silicon "fin", which forms the body of the device. The off state subthreshold current is much less.



http://en.wikipedia.org/wiki/File:Doublegate_FinFET.PNG



Triple and stacked multi-gate structure, for increasing integration level

Special cases for digital memories:

- In the memory space memristors are gaining importance. The technology is considered faster than classic flash technologies, also drawing low power. Solid state memory already lowers the amount of power being used due to there are no moving parts, but memristor reportedly uses as little as one tenth the power of flash.

Collection of solutions and the technology node when it was introduced and their effect.

Feature	Typical node	Effect
Copper routing	150 nm	Increase performance
Low-K dielectic	130 nm	Increase performance Reduce power
Multi-threshold transistors	90 nm	Reduce power
Triple gate oxide	65 nm	Reduce power
Strained silicon	65 nm	Increase performance

Section III

Soft solutions to reduce power consumption

System level concerns

- Power consumption is heavily application-dependant. The same processor would show different power characteristics when used in a CD player and in a cellular phone.
- Low power design techniques could be applied at various levels during the design cycle, from specification to physical integration and tapeout:
  - Architecture definition,
  - RTL definition and coding,
  - Gate level implementation, and
  - Transistor Level implementation
- The vast majority of power saved at higher levels!

Reducing the static consumption

- With the scaling down, the static consumption's components changes as well.
- Decrease in junction area and voltage automatically decreases junction reverse bias leakage and the gate induced drain leakage (I_{REV}, I_{GIDL}).
- Designer has a little control over threshold voltage!

The subthreshold region starts when V_{drain}-V_{gate} > $4kT/q \sim 100$ mV. In this mode, the current is estimated as:

$$I \sim I_0 \exp((V_{gate}-V_{substrate})/V_{threshold})$$

The possible methods to have control over these leakage components is to switch off the device itself in controlled fashion:

- Clock gating
- Power gating
- Back biasing of the substrate around the transistor.
- Mix of different threshold voltage type transistors where available in a controlled, adaptive way

Clock gating

- The switching activity results in dynamic consumption. To save power, clock gating can be applied. This method adds more logic to a circuit to prune the clock tree, thus disabling portions of the circuitry.

Power gating

- Power gating is a technique wherein circuit blocks that are not in use are temporarily turned off, put in "low power mode“.
- Adding a sleep transistor to every cell that is to be turned off imposes a large area penalty and rarely used.
- Isolation cells are used to prevent short circuit current.

Back biasing for controlling the speed/leakage ratio as multi-threshold transistors

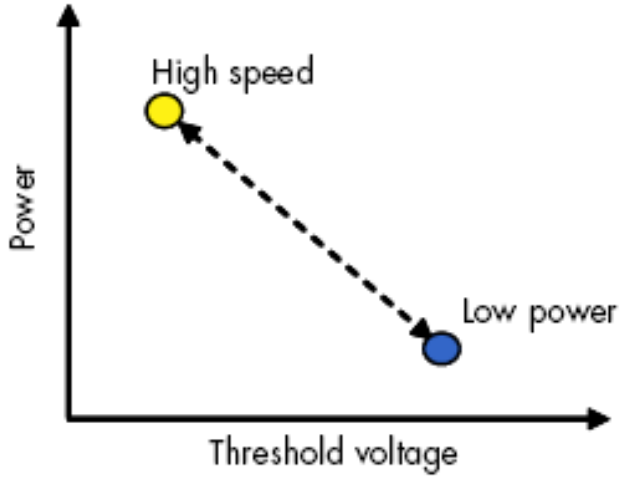
- The transistor's substrate are formed in separated wells, of which potential are independently controlled. For an NMOS, this would mean applying a negative voltage to the P-Well relative to the zero source potential. This bias has the effect of shifting the threshold voltage.
- Difficult circuit solution as we have to generate and control negative voltages.

Back biasing

- In non-timing-critical circuit paths low-power mode can be applied.
- If we reduces the back bias voltage (making it more negative), which closes the transistor more, and makes it difficult to turn on. This minimizes subthreshold leakage currents and unwanted static power.

Back biasing

- In high-performance mode, when a few timing-critical paths needs quicker operation to help meet the design's specified timing constraints and deliver maximum performance, we can increase the back bias voltage (making it less negative), which makes the transistor easier to turn on.



Section IV

CAD tool support for automated power consumption optimization

CAD tool support

- Most of the low-power design tools and standard cell libraries are well-established and supported the basic techniques such as
  - Power and clock gating for reducing static and dynamic power
  - multiple voltage thresholds (multi-Vt) to decrease leakage current by existing tools for a single mode/corner combination
- Difficulties come with more-advanced techniques such as designing for power in a multi-corner multi-mode (MCMM) situation, multi-voltage flows, and designing power efficient clock trees.
- Handling of separated voltage islands are also supported.

CAD tool support

- In a multi-corner multi-mode scheme, clock power consumption depends on various factors such as clock driver sizing, clock distribution wiring, the circuit design style, architectural choice, and the capability to disable part of the clocking network.
- The existing voltage islands makes the timing and power analyis even time consuming, as they generates a lot of new min/max voltage combinations.

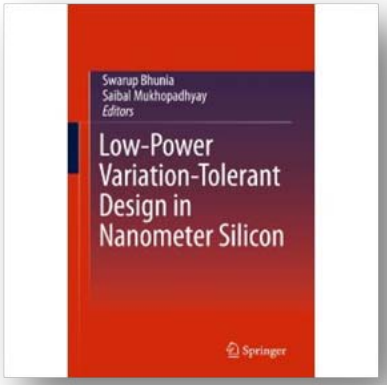
Example:

- The Phoenix Processor (2008), is intended for use in sensor-based devices such as medical implants, environment monitors, which can spend more than 99 percent in sleep mode.
- The chip consumes 30 pW during sleep mode (263 years operation time with a watch battery), 300 nW in operation.
- Solution:
  - Power supply is 0.5V (at 180 nm the standard is 1.8V), power gating, low leakage memory cells, low voltage ROM
  - CPU with compact ISA
  - data memory compression, and adaptive data memory leakage management.

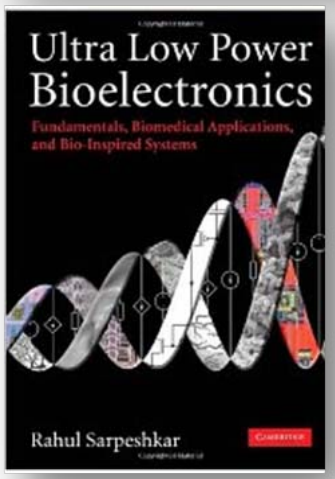
Conclusions

- The power consumption increases exponentially with scaling down, due to technological and increasing integration level
- The handling of power consumption became a critical issue, many time, more important than speed.
- Several technological and system level design solutions are developed to mitigate it.

Recommended literature



Low-Power Variation-Tolerant Design in Nanometer Silicon
Swarup Bhunia, Saibal Mukhopadhyay
Springer; 1st Edition. edition



Ultra Low Power Bioelectronics: Fundamentals, Biomedical Applications, and Bio-Inspired Systems
Rahul Sarpeshkar
Cambridge University Press; 1st edition (February 22, 2010)

Comprehension questions:

I. Why circuits consume power?

II. What is dynamic and static power consumption?

III. Describe technological solutions to reduce power consumption.

IV. Describe architectural and software solutions to reduce power consumption.